

04feb04 14:25:49 User267149 Session D1226.1

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2004/Jan W4

(c) 2004 Institution of Electrical Engineers

\*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.

File 6:NTIS 1964-2004/Feb W1

(c) 2004 NTIS, Intl Cpyrght All Rights Res

File 8:Ei Compendex(R) 1970-2004/Jan W4

(c) 2004 Elsevier Eng. Info. Inc.

File 34:SciSearch(R) Cited Ref Sci 1990-2004/Jan W4

(c) 2004 Inst for Sci Info

\*File 34: New prices as of 1/1/2004 per Information Provider request. See HELP RATES 34.

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

(c) 1998 Inst for Sci Info

\*File 434: New prices as of 1/1/2004 per Information Provider request. See HELP RATES434.

File 35:Dissertation Abs Online 1861-2004/Jan

(c) 2004 ProQuest Info&Learning

File 65:Inside Conferences 1993-2004/Feb W1

(c) 2004 BLDSC all rts. reserv.

File 94:JICST-EPlus 1985-2004/Jan W4

(c)2004 Japan Science and Tech Corp(JST)

File 99:Wilson Appl. Sci & Tech Abs 1983-2004/Dec

(c) 2004 The HW Wilson Co.

File 144:Pascal 1973-2004/Jan W4

(c) 2004 INIST/CNRS

File 305:Analytical Abstracts 1980-2004/Dec W4

(c) 2004 Royal Soc Chemistry

\*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.

File 315:ChemEng & Biotech Abs 1970-2004/Jan

(c) 2004 DECHEMA

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200408

(c) 2004 Thomson Derwent

\*File 350: New prices as of 1-1-04 per Information Provider request. See HELP RATES350

File 347:JAPIO Oct 1976-2003/Sep(Updated 040105)

(c) 2004 JPO & JAPIO

\*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.

File 344:Chinese Patents Abs Aug 1985-2003/Nov

(c) 2003 European Patent Office

File 371:French Patents 1961-2002/BOPI 200209

(c) 2002 INPI. All rts. reserv.

\*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	5181	(UNITARY OR UNIT? ?) (3N) (CAPACITOR? ? OR WINDOWFRAM? OR WINDOW() FRAM?)
S2	9537	CAPACITOR? ?(3N) (PLASTIC? OR STACK??? OR MOUNT????????? OR - FILE???)
S3	14582	S1:S2
S4	347121	(BOTTOM OR TOP OR LOWER OR HIGHER) (3N) SURFACE? ?
S5	4069806	APERTUR? OR HOLE? ? OR GAP? ? OR SLIT? ? OR OPENING? ?
S6	21316	(APERTUR? OR HOLE? ? OR GAP? ? OR SLIT? ? OR OPENING? ?) (3-N) RECTANGULAR????
S7	4069806	S5:S6
S8	190520	ELECTRICAL?????? (3N) CONNECT??????
S9	23988660	SUBSTRAT? OR SURFACE? OR BASE? OR SUBSTRUCT? OR UNDERSTRUCT? OR UNDERLAY? OR FOUNDATION? OR PANE? OR DISK? OR DISC? OR - WAFER?
S10	28	UNCOVER????? (3N) PERIPHERAL???
S11	24172	PERIPHERAL??? (3N) PORTION? ?
S12	24198	S10:S11
S13	7852	SEMICONDUCT?????? (3N) (DIE OR DIED OR DIEING OR DIES OR DICE OR CUT OR CHOP???)
S14	17457	BALL? ?(3N) (GRID OR ARRAY) OR BALL() GRID() ARRAY OR BGA
S15	9734	SOLDER? (3N) BALL? ?
S16	23317	S14:S15
S17	3587219	CONDUCT??????
S18	2201	S3 AND S7
S19	1534	S18 AND S9
S20	153	S19 AND S8
S21	15	S20 AND S4
S22	15	RD (unique items)
S23	138	S20 NOT S21
S24	1	S23 AND S12
S25	137	S23 NOT S24
S26	1	S25 AND S13
S27	136	S25 NOT S26
S28	2	S27 AND S16
S29	134	S27 NOT S28
S30	66	S29 AND S17
S31	22	S20 AND S1
S32	0	S31 AND S6
S33	22	RD S31 (unique items)
S34	2560	S3 AND S17
S35	9	S34 AND S16
S36	8	RD (unique items)
S37	7	S36 NOT S21, S24, S26, S28
S38	4989	S16 AND S7
S39	416	S38 AND CONDUCTOR? ?
S40	0	S39 AND S3
S41	5	S39 AND CAPACITOR? ?
S42	5	RD (unique items)
S43	411	S39 NOT S41
S44	355	S43 AND S9
S45	16	S44 AND S13
S46	16	S45 NOT S21, S24, S26, S28, S36

015626453

WPI Acc No: 2003-688624/200365

22/3,AB/1

(Item 1 from file: 350)

XRAM Acc No: C03-188726

XRPX Acc No: N03-550189

Semiconductor memory device includes **stack-shaped capacitor** having two electrodes and dielectric layer, where bit line and MOS transistors in cell area are disposed beneath the capacitor, guard-ring pattern, and contact fill

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU ); KIM K (KIMK-I); PARK B (PARK-I)

Inventor: KIM G N; PARK B J; KIM K; PARK B

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030132429	A1	20030717	US 2002246392	A	20020919	200365 B
KR 2003062087	A	20030723	KR 20022509	A	20020116	200381

Priority Applications (No Type Date): KR 20022509 A 20020116

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030132429	A1	21	H01L-047/00	
KR 2003062087	A		H01L-027/108	

Abstract (Basic): US 20030132429 A1

Abstract (Basic):

NOVELTY - Semiconductor memory device comprises:

(i) a **stack-shaped capacitor** comprising a first electrode, a dielectric layer, and a second electrode, where bit line and MOS transistors in a cell area are disposed beneath the **stack-shaped capacitor**;

(ii) a guard-ring pattern between the cell area and the peripheral circuit area; and

(iii) a contact fill for a plate electrode formed in the guard-ring pattern and in contact with the second electrode

DETAILED DESCRIPTION - Semiconductor memory device comprises:

(a) an oxide layer for isolating individual devices which define device areas so that a cell area and a peripheral circuit area are separated from each other on a semiconductor **substrate**;

(b) metal oxide semiconductor (MOS) transistors comprising source areas, drain areas, and gates that are formed in the cell area and the peripheral circuit area;

(c) a bit line (120) formed on the MOS transistors and **electrically connected** to the MOS transistor;

(d) a **stack-shaped capacitor** comprising a first electrode, a dielectric layer, and a second electrode, where the bit line and the MOS transistors in the cell area are disposed beneath the **stack-shaped capacitor**;

(e) a guard-ring pattern interposed between the cell area and the peripheral circuit area, surrounding the cell area and spaced apart from the peripheral circuit area; and

(f) a contact fill (110) for a plate electrode formed in the guard-ring pattern (151b) and in contact with the second electrode.

The second electrode is formed on the internal sidewall and the bottom of the guard-ring pattern.

An INDEPENDENT CLAIM is also included for a method for manufacturing a semiconductor memory device, which comprises:

- (1) separating a cell area from a peripheral circuit area on a semiconductor **substrate** and forming device active areas;
- (2) forming MOS transistors in the device active areas;
- (3) forming a first interlayer dielectric (ILD) film (105) on the **substrate** and forming a first electrode pattern and a guard-ring pattern surrounding the cell area on the first ILD film;
- (4) sequentially forming a conductive layer (121) for a first electrode and an insulating layer (123) for patterning on the first electrode pattern and the guard-ring pattern;
- (5) **opening** the cell area and a part of the guard-ring pattern, removing the conductive layer for the first electrode and the insulating layer for patterning to the first ILD film, and forming a first electrode node in the cell area;
- (6) removing the insulating layer for patterning that is filled in the first electrode node;
- (7) forming a dielectric layer and a conductive layer for a second electrode on the **substrate**;
- (8) forming a pattern for a second electrode on the conductive layer for the second electrode; and
- (9) forming a contact fill for a plate electrode while in contact with the second electrode that is formed on the sidewall and the bottom of the guard-ring pattern.

USE - The semiconductor memory device is used as, i.e. dynamic random access memory device.

ADVANTAGE - A wide contact area is formed on a plate electrode for serving as the ground electrode of a capacitor so that a step between a cell area of a semiconductor chip and a peripheral area formed by a capacitor formed in the cell area is effectively decreased, thus greatly reducing ground resistance and improving the electric characteristics of a memory device.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view illustrating a method for manufacturing a semiconductor memory device.

First interlayer dielectric film (105)

Contact fill (110)

Bit line (120)

Conductive layer (121)

Insulating layer (123)

Guard-ring pattern (151b)

pp; 21 DwgNo 2/10

22/3,AB/2 (Item 2 from file: 350)  
 DIALOG(R)File 350:Derwent WPIX  
 (c) 2004 Thomson Derwent. All rts. reserv.

015136071

WPI Acc No: 2003-196597/200319

XRAM Acc No: C03-050602

XRPX Acc No: N03-155917

Method for fabricating **stacked capacitors** in a memory device

- capable of reducing the dimension of the capacitor while maintaining the capacitance

Patent Assignee: VANGUARD INT SEMICONDUCTOR CORP (VANG-N)

Inventor: TZENG H

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
TW 484231	A	20020421	TW 2000121076	A	20001009	200319 B

Priority Applications (No Type Date): TW 2000121076 A 20001009

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes  
TW 484231 A H01L-027/108

Abstract (Basic): TW 484231 A

Abstract (Basic):

NOVELTY - There is provided a method for fabricating **stacked capacitors** in a memory device, which comprises providing a **substrate** formed thereon several conductive structures, each having a cap layer on the top; forming a dielectric layer on the **substrate** and conductive structures; defining the dielectric layer to form an **opening** among the conductive structures for exposing the **substrate**, the sidewall of the conductive structure, and part of the **top surface** of the conductive structure; filling the **opening** by a conductive plug and forming a dielectric block thereon; forming a conductive spacer on the sidewall of the dielectric block to be **electrically connected** to the conductive plug; removing the dielectric block to expose the conductive plug; forming a hemi-spherical grain conductive layer on the topography **surface** of the **substrate**; forming a dielectric spacer on the sidewall of the conductive spacer to cover part of the hemi-spherical grain conductive layer, wherein the dielectric spacer includes material with different etching selectivity with respect to the dielectric layer; removing the hemi-spherical grain conductive layer not covered by the dielectric spacer by etching-back process; removing the dielectric spacer; and forming a second dielectric layer and capacitor electrode layer on the **substrate**.

DwgNo 1/1

22/3,AB/3 (Item 3 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

014470672

WPI Acc No: 2002-291375/200233

XRAM Acc No: C02-085449

XRPX Acc No: N02-227508

Fabrication of self-aligned **stacked capacitor** involves forming **opening** on second insulation layer, etching stop layer and third insulation layer, and forming first conductive layer on interior **surface of opening**

Patent Assignee: UNITED MICROELECTRONICS CORP (UNMI-N)

Inventor: LEE C; LIAO W; YANG K

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020022321	A1	20020221	US 2000621923	A	20000724	200233 B
			US 2001971542	A	20011005	
US 6413817	B1	20020702	US 2000621923	A	20000724	200248
			US 2001971542	A	20011005	

Priority Applications (No Type Date): US 2000621923 A 20000724; US 2001971542 A 20011005

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes  
US 20020022321 A1 11 H01L-021/8242 Div ex application US 2000621923  
US 6413817 B1 H01L-021/8242 Div ex application US 2000621923

Abstract (Basic): US 20020022321 A1

Abstract (Basic):

**NOVELTY** - A self-aligned **stacked capacitor** is fabricated by forming an **opening** on a second insulation layer, an etching stop layer and a third insulation layer. A first conductive layer is formed on an interior **surface** of the **opening** to form a second section node contact. A bottom and an upper portion of first conductive layer respectively form a bottom and a crown-shaped section of a lower electrode.

**DETAILED DESCRIPTION** - Fabrication of a self-aligned **stacked capacitor** involves providing a **substrate** (500) having a first insulation layer (555). A bit line contact and a first section node contact (570) are formed through the first insulation layer, and bit line structure (586) is formed above the first insulation layer. The bit line structure includes a bit line, a cap layer, and spacers. The bit line **electrically connects** with the bit line contact. The cap layer is above the bit line, and the spacers are on sidewalls of the bit line and the cap layer. A second insulation layer (590), an etching stop layer (600), and a third insulation layer (610) are sequentially formed on the **substrate**. An **opening** (625) is formed through the second insulation layer, the etching stop layer, and the third insulation layer to expose a portion of the bit line structure and the first section node contact. A conformal first conductive layer is formed on an interior **surface** of the **opening** to form a second section node contact (630b). A bottom portion of the first conductive layer forms a bottom section of a lower electrode (630a), and an upper portion of the first conductive layer forms a crown-shaped section of the lower electrode. A conformal dielectric layer (650) and a second conductive layer (660) are sequentially formed on the **substrate**. The second conductive layer forms an upper electrode of the **stacked capacitor**.

**USE** - For the fabrication of self-aligned **stacked capacitor** used in dynamic random access memory cell.

**ADVANTAGE** - The inventive method provides self-aligned **stacked capacitor** capable of reducing processing complexity and pollution due to micro-particles. It prevents short-circuiting between the bit line and the second section node contact, without requiring the formation of a silicon nitride liner layer on the sidewalls of the second section node contact **opening**. The aspect ratio in subsequent contact **opening** etching process is decreased, and a higher tolerance for the contact **opening** is obtained.

**DESCRIPTION OF DRAWING(S)** - The figure shows a cross-sectional view of the crown-shaped capacitor.

**Substrate** (500)

First insulation layer (555)

First section node contact (570)

Bit line structure (586)

Second insulation layer (590)

Etching stop layer (600)

Third insulation layer (610)

**Opening** (625)

Lower electrode (630a)

Second section node contact (630b)

Hemispherical silicon grains (640)

Dielectric layer (650)

Second conductive layer (660)

pp; 11 DwgNo 9/10

(c) 2004 Thomson Derwent. All rts. reserv.

014428030

WPI Acc No: 2002-248733/200230

XRPX Acc No: N02-193134

Electrode structure for **electrical** storage device, **connects**  
heteropolar portions of stacking electrode by attaching connecting plate  
over adjacent frame

Patent Assignee: NISSAN DIESEL KOGYO KK (NSMO )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2002050539	A	20020215	JP 2000238081	A	20000807	200230 B

Priority Applications (No Type Date): JP 2000238081 A 20000807

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2002050539	A	5	H01G-004/228	

Abstract (Basic): JP 2002050539 A

Abstract (Basic):

NOVELTY - A set of rectangular parallelepiped shaped frames (5) is  
moved along specific direction, through a pair of connection grooves  
(9,9a) into an **opening** of an insulated board (3). The like poles  
of the stacking electrodes (8) of a capacitive portion are piled on  
**top** of the bearing **surface** of a frame. The heteropolar  
portions of the stacking electrode are connected by attaching a  
connecting plate (6) over the adjacent frame.

USE - For electrical storage device.

ADVANTAGE - Reduces contact resistance between electrodes, and  
balances electrode lengths, thus improving quality of component.  
Reduces number of components such as frame and connecting plate,  
thereby reducing cost. Simplifies attachment of frames. Increases  
storage capacity by **stacking** required number of **capacitors**.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view  
indicating the electrode structure.

Insulated board (3)

Frames (5)

Connecting plate (6)

Stacking electrodes (8)

Connection grooves (9,9a)

pp; 5 DwgNo 4/11

22/3,AB/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

013795555

WPI Acc No: 2001-279766/200129

XRAM Acc No: C02-058461

XRPX Acc No: N02-143136

Fabrication of **stacked capacitor** by forming interlayer  
insulative and lower conductive seed layers, forming non-conductor  
patterns, and simultaneously forming buried contacts and lower electrodes  
by lower electroplating process

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU )

Inventor: HORI H; HORII H

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2000066883	A	20001115	KR 9914272	A	19990421	200129 B
US 6255187	B1	20010703	US 2000551524	A	20000418	200225
KR 289739	B	20010515	KR 9914272	A	19990421	200223

Priority Applications (No Type Date): KR 9914272 A 19990421

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2000066883	A			H01L-029/92	
US 6255187	B1	17		H01L-021/20	
KR 289739	B			H01L-029/92	Previous Publ. patent KR 2000066883

Abstract (Basic): US 6255187 B1

Abstract (Basic):

NOVELTY - A **stacked capacitor** is made by:

(a) forming a lower conductive seed layer over innerwalls of buried contact **holes** and an upper **surface** of an interlayer insulative layer;

(b) forming non-conductor patterns over the lower seed layer and the upper **surface**; and

(c) simultaneously forming buried contacts and lower electrodes by a lower electroplating process

DETAILED DESCRIPTION - Fabrication of a **stacked capacitor** includes preparing a semiconductor **substrate** (10) having exposed conductive areas.

An interlayer insulative layer (20) is formed over the **substrate**, and has buried contact **holes** that expose the conductive areas.

A lower conductive seed layer is formed over innerwalls of the buried contact **holes** and an upper **surface** of the interlayer insulative layer.

Non-conductor patterns are formed over the lower conductive and the upper **surface** of the interlayer insulative layer. They have storage node **holes** that expose the buried contact **holes**.

Buried contacts (72) that fill the buried contact **holes** and lower electrodes (74) that fill the storage node **holes** are simultaneously formed by a lower electroplating process.

USE - For fabricating a **stacked capacitor**.

ADVANTAGE - The method does not need to form a barrier layer between the buried contact and the lower electrode. It does not require dry etching of the conductive layer to separate the storage nodes when the lower electrode is formed of a conductive film, e.g. metal of the platinum group. It does not have misalignment problems between the buried contact and the lower electrode.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of fabricating a **stacked capacitor**.

**Substrate** (10)

Pads (12)

Interlayer insulative layer (20)

Barrier layer (32)

Buried contacts (72)

Lower electrodes (74)

Dielectric layer (80)

Upper electrode (90)

pp; 17 DwgNo 1H/6

(c) 2004 Thomson Derwent. All rts. reserv.

010662860

WPI Acc No: 1996-159814/199616

XRPX Acc No: N96-133916

Integrated circuit with capacitive decoupling for eliminating inductively induced delay - has integrated circuit element contained within integrated circuit casing with **aperture** extending through casing upper and **lower surface** adapted partially to receive **discrete** electrical circuit element

Patent Assignee: STAKTEK CORP (STAK-N)

Inventor: BURNS C D; ROANE J M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5498906	A	19960312	US 93153511	A	19931117	199616 B

Priority Applications (No Type Date): US 93153511 A 19931117

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5498906	A	14	H01L-023/02	

Abstract (Basic): US 5498906 A

The package comprises an integrated circuit element contained within an integrated circuit casing which has an upper **surface**, **lower surface** and perimeter wall. The casing includes an **aperture** (10) which extends completely through the upper and **lower casing surfaces** and is adapted to partially receive a **discrete** electrical circuit element comprising a bypass capacitor (12).

The electrical circuit element has one lead **electrically connected** to a power supply input and the other lead **electrically connected** to a ground input for the integrated circuit element. The capacitor attachment leads are brought out of the IC package in such a way that when capacitors are attached to alternating positions, the individually packaged IC's can be stacked into modules without increasing the vertical height of the module.

USE/ADVANTAGE - For memory IC devices. Eliminates inductively induced delay. Alternate vertical stacking technique eliminates interference between bypass **capacitor** of each **stacked** IC device and improves stack-ability. Improves power supply decoupling and reduces ground bounce and provides additional improvement to clock-data access time for memory devices. Provides increased noise margin.

Dwg.1/8

22/3,AB/7 (Item 7 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

009626674

WPI Acc No: 1993-320223/199340

Related WPI Acc No: 1993-167174

XRPX Acc No: N93-246725

Semiconductor device package with solder bump **electrical connections** - has exterior wells to contain capacitors, beneath which are cleaning channels for removing residual flux and-or solder

Patent Assignee: LSI LOGIC CORP (LSIL-N)

Inventor: LEY T; ROSTOKER M D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5249098	A	19930928	US 91749128	A	19910822	199340 B
			US 92922118	A	19920728	

Priority Applications (No Type Date): US 92922118 A 19920728; US 91749128 A 19910822

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5249098	A	10	H02B-000/00	CIP of application US 91749128

Abstract (Basic): US 5249098 A

The package comprises a body having length, width and breadth and occupying a spatial volume, and having a flat exterior **surface**. A die-receiving **opening** extends into the flat exterior **surface** of the body. At least one capacitor-receiving **opening** extends into the flat exterior **surface** of the body, separate and distinct from the die-receiving **opening**.

A capacitor is disposed at least partially within each of the at least one capacitor-receiving **openings**. Solder bump **electrical connections** are provided on the **bottom surface** of the flat exterior **surface** of the body.

USE/ADVANTAGE - For **mounting** external **capacitors**, with shorter lead length, in manner to allow for better cleaning of flux and solder balls, improving mfg. yield.

Dwg.7/7

22/3,AB/8 (Item 8 from file: 350)  
 DIALOG(R)File 350:Derwent WPIX  
 (c) 2004 Thomson Derwent. All rts. reserv.

008563069

WPI Acc No: 1991-067104/199110

XRAM Acc No: C91-028356

XRPX Acc No: N91-051926

Semiconductor memory device - has fin-type **stacked** charge storage **capacitor**

Patent Assignee: FUJITSU LTD (FUIT )

Inventor: GOTOU H

Number of Countries: 006 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 415530	A	19910306	EP 90307353	A	19900705	199110 B
JP 3038061	A	19910219				199113
US 5126810	A	19920630	US 90547368	A	19900703	199229
			US 91742261	A	19910807	
US 5196365	A	19930323	US 90547368	A	19900703	199314
			US 91742261	A	19910807	
			US 91779548	A	19911018	
EP 415530	B1	19941130	EP 90307353	A	19900705	199501
KR 9401020	B1	19940208	KR 9010181	A	19900705	199502
DE 69014486	E	19950112	DE 614486	A	19900705	199507
			EP 90307353	A	19900705	

Priority Applications (No Type Date): JP 89171827 A 19890705

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
EP 415530	A			

Designated States (Regional): DE FR GB

US 5126810 A H01L-029/68 Cont of application US 90547368

US	5196365	A	30	H01L-021/70	Div ex application US 90547368
					Cont of application US 91742261
EP	415530	B1 E	41	H01L-027/108	
				Designated States (Regional): DE FR GB	
DE	69014486	E		H01L-027/108	Based on patent EP 415530
KR	9401020	B1		H01L-027/108	

Abstract (Basic): EP 415530 A

A semiconductor memory device, having a fin-type **stacked** charge storage **capacitor**, comprises a **substrate** (1), a transfer transistor including drain and source (6.1, 6.2, 5), and with a charge storage capacitor electrode coupled to one of these via a conductive **base** layer (15.1). The capacitor also comprises a conductive side wall (22) connected to one end of the **base**, and having many fins (15.2, 15.3) extending parallel to the **base**, a dielectric layer (24) covering **base**, side wall and fins, and a conductive layer (25) on the dielectric layer forming the opposed electrode of the capacitor. The fins and side wall form a storage electrode.

Also claimed is prodn. of the device in which first and second layers (15.1-15.3) are alternately formed on an insulator layer (3) to give a stack, at least the first layers being conductive and the lowest coupled to the source/drain. The side wall is formed, the second layers of the stack removed and the dielectric (24) and conductor (25) layers formed. Further claimed is prodn. of the device comprising forming gate insulator (3), word line (4) and interlayer insulator (7) on the **substrate** (1), forming contact **holes** to source/drain, forming and patterning first and second layers, and forming a side wall (22) and dielectric and conductor layers as above. A second interlayer insulator (26) is formed on the conductor, a third contact **hole** formed, followed by a second conductive layer forming a bit line (27).

ADVANTAGE - Capacitance is three times that of other capacitors of this type, the fins do not break easily and capacitor alignment is simple. Breakage of the bit line at the contact **hole** is prevented. (36pp Dwg.No 28B/28)ng

Abstract (Equivalent): EP 415530 B

A semiconductor memory device including a transfer transistor having first and second regions (5) constituting respectively source and drain regions of the transistor, which regions are formed in a **substrate** (1) of the device at a main **surface** of the **substrate**; an insulator layer (2,3) formed on the said main **surface**; a first conductive layer contacting one of the said active regions, so as to be **electrically connected** therewith, through a contact **hole** formed in the said insulator layer (2,3) and extending outwardly beyond the periphery of the contact **hole** so as to overlap the said insulator layer (2,3) adjacent to the **hole**; at least one further conductive layer located above the said first conductive layer, and extending generally parallel thereto, to form a stack in which the conductive layers are spaced apart one from the next and **connected electrically** together to form a first electrode structure of a charge storage capacitor of the device; and conductive material provided around the said stack, and within the spaces between the adjacent conductive layers thereof, to form a second electrode structure of the charge storage capacitor, which second electrode structure is separated from the said first electrode structure by a dielectric covering layer on the first electrode structure; characterised by a side wall structure made of conductive material and formed alongside the said stack so as to be connected physically to mutually-corresponding respective outer edge regions, remote from the said contact **hole**, of the conductive layers, so

that the said conductive layers together with the said side wall structure constitute the said first electrode structure.

(Dwg.1/28

Abstract (Equivalent): US 5196365 A

Process comprises alternately forming 1st and 2nd layers several times on a **substrate** to form a stacked structure above one of source and drain regions of the transfer transistor. The 1st layer is a conductive material, the lower most of the 1st layers being electrically coupled to the source and drain region via a contact **hole** in the insulator layer. Stacked structure is patterned and side wall is formed on one side. The 2nd layer is removed and dielectric layer formed on exposed **surfaces** of the 1st layers and side wall. Conductive layer is formed on the dielectric layer **surface** to form an opposed electrode of the charge storage capacitor.

ADVANTAGE - Semiconductor memory device has fin type stacked structure used as charge storage capacitor.

om

Dwg.17b/28

US 5126810 A

Semiconductor memory device comprises a) a **substrate**; b) a transfer transistor formed on a) and including drain and source regions; and c) a charge storage capacitor electrically coupled to one of the drain and source regions of transistor b) Capacitor c) includes i) a conductive **base** layer having a **bottom surface** which is electrically coupled to one of the drain and source regions of transistor b) at a central part of layer i), layer i) having outward extending portions extending outwardly from the **bottom surface** in all directions from the central part; ii) at least one conductive side wall connected to one end of one outward extending portion of layer i); iii) fin-shaped parts which extend from the side wall in levels generally parallel to layer i) and exist above the central part of layer i); iv) a dielectric layer which covers exposed **surfaces** of layer i), the side wall and fin-shaped parts; and v) a conductor layer which is formed on layer iv) to form an opposed electrode of capacitor c). Layer i), the fin-shaped parts and the side wall form a storage electrode of capacitor c).

ADVANTAGE - New device has a charge storage capacitor having a capacitance about three times that of conventional fin type charge storage capacitor.

Dwg.17b/28

22/3,AB/9.. (Item 9 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

008136841

WPI Acc No: 1990-023842/199004

XRPX Acc No: N90-018262

Storage device with high packing density - has DRAM with layered capacitor cell and transfer gate transistor and capacitor

Patent Assignee: MITSUBISHI DENKI KK (MITQ )

Inventor: WAKAMIYA W; OGOH I

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3922456	A	19900111	DE 3922456	A	19890707	199004 B
JP 2021652	A	19900124	JP 88171523	A	19880708	199010
US 5101251	A	19920331	US 89376660	A	19890707	199216

Priority Applications (No Type Date): JP 88171523 A 19880708

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
-----------	------	-----	----	----------	--------------

DE 3922456	A		13		
------------	---	--	----	--	--

US 5101251	A		12		
------------	---	--	----	--	--

DE 3922456	C2		11	H01L-027/108	
------------	----	--	----	--------------	--

Abstract (Basic): DE 3922456 A

The storage device has an arrangement of memory cell units each with a switch (13). A conducting film (15) is formed at a given region (5a) of the switch (13). At least one section of the first electrode layer (8) of the passive signal-storing element (14) is connected to the conducting film.

One section of a **bottom surface** of the concave section (12) is formed in the insulating film (16) is arranged on one **surface** of a given region (5a) of the switch (13) to which the first electrode layer (8) of the storage element (14) is **electrically connected**.

USE - DRAM.

1/9

Abstract (Equivalent): DE 3922456 C

An oxide film separates each cell. This transistor possesses a first and second zone (5a,5b) of impurity in the **substrate** (1), some distance apart, and a first conducting layer (4a) enclosed by insulating material (3,6) and formed between the zones of impurity on the **surface** of the **substrate**. On the first impurity zone a conducting film (15) extends to an upper section of the first conducting layer and to an upper section of the oxide film and there is an insulating film (16) with a flat **surface** and with an **opening** (12) in the **substrate** stretching to the conducting film. The capacitor (14) is formed on the **surface** of the insulating film (10). A dielectric film (10) and a first electrode layer are connected to the conducting film. A second electrode layer (11) is in contact with the dielectric film. ADVANTAGE - By miniaturising the structures degree of integration is enhanced, and capacity of the capacitor increased. (Dwg.1/7)

Abstract (Equivalent): US 5101251 A

The DRAM having **stacked capacitor** cell comprises one transfer gate transistor and one capacitor. A thick insulating film having flat **surface** is formed on the **surface** of the transfer gate transistor and the like. A conductive film is formed on a **surface** of one impurity region of the transfer gate transistor. An **opening** portion deep enough to reach the conductive film is formed in the insulating film. The capacitor is formed in the **opening** portion and on the upper **surface** of the insulating film. A lower electrode of the capacitor is connected to the conductive film. An insulating film having a flat **surface** is formed by a reflow process employing thermal processing, plasma ECR CVD method and the like. ADVANTAGE - Improved degree of integration and miniaturisation

22/3,AB/10 (Item 10 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

007513460

WPI Acc No: 1988-147393/198821

Electronic packaging structure - of thin structure carrying chips mounted on second level electronic package with chips in package **opening**

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC ); IBM CORP (IBMC )

Inventor: BLACK V J; CHARSKY R S; OLSON L T

Number of Countries: 006 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4744008	A	19880510	US 8797322	A	19870911	198821 B
EP 268260	A	19880525	EP 87116952	A	19871117	198821
JP 63131561	A	19880603	JP 87231256	A	19870917	198828
EP 268260	B1	19920805	EP 87116952	A	19871117	199232
DE 3780915	G	19920910	DE 3780915	A	19871117	199238
			EP 87116952	A	19871117	

Priority Applications (No Type Date): US 86931813 A 19861118; US 8797322 A 19870911

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
-----------	------	-----	----	----------	--------------

US 4744008	A		7		
------------	---	--	---	--	--

EP 268260	A	E			
-----------	---	---	--	--	--

Designated States (Regional): DE FR GB IT

EP 268260	B1	E	7	H01L-023/58	
-----------	----	---	---	-------------	--

Designated States (Regional): DE FR GB IT

DE 3780915	G			H01L-023/58	Based on patent EP 268260
------------	---	--	--	-------------	---------------------------

Abstract (Basic): US 4744008 A

Second level electronic package has one **opening** for accommodating a semiconductor chip and having circuitry for **electrical connection** to the chip. A circuitised thin film structure has a semiconductor chip mounted on one side of the thin film structure and at least one decoupling **capacitor mounted** on an opposite side of the thin film structure which is **electrically connected** to input/output contacts of the chip. The thin film structure is mounted on the second level electronic package with the semiconductor chip positioned in the **opening** of the second level package and with the circuitry on the thin film structure connected to the circuitry on the second level electronic package to electrically interconnect in the input/output contacts of the semiconductor chip to the circuitry on the second level electronic package.

USE/ADVANTAGE - Partic. to a semiconductor chip carrier first level electronic packages having high freq. decoupling capacitors as part of the package. Assembly reduces the noise associated with the increase in the rate at which the current switches, minimises the inductance paths and maximises the wireability of the **top surface** of the carrier associated with the semiconductor chip.

1/2

Abstract (Equivalent): EP 268260 B

An electronic packaging structure comprising: a ceramic card (12) having at least one cavity (14) therein for accommodating a semiconductor chip and having circuitry (20) for **electrical connection** to the said semiconductor chip; and a thin circuitized film structure (26) consisting of a polyimide film chip carrier (28) provided with vias (38) supporting at least one metal pattern (30) on one side; at least one semiconductor chip (24) mounted on said one side of the film structure, the input/output contacts (32) of said chip being **electrically connected** to said metal pattern (30); at least one decoupling **capacitor** (34) **mounted** on the opposite side of the film structure and **electrically connected** to the input-output contacts (32) of said semiconductor chip (24) through said vias (38); said film structure being mounted on said ceramic card

with the semiconductor chip positioned in said cavity and with the metal pattern (30 of said film structure (26) connected to the circuitry (20) of said ceramic card.

(Dwg./3

22/3,AB/11 (Item 11 from file: 350)  
DIALOG(R) File 350:Derwent.WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

004261355

WPI Acc No: 1985-088233/198515

XRPX Acc No: N85-066015

Noise suppression filter with ferrite block - has strip electrode through longitudinal **hole**, with ends bent over to contact capacitors on top

Patent Assignee: MURATA MFG CO LTD (MURA )

Inventor: FUJIKI Y; HORI T

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 3432670	A	19850404	DE 3432670	A	19840905	198515 B
US 4571561	A	19860218	US 84645310	A	19840829	198610
DE 3432670	C	19890105				198902

Priority Applications (No Type Date): JP 83U138656 U 19830905

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3432670	A		23		

Abstract (Basic): DE 3432670 A

The filter has a rectangular block (20) of ferrite material with a longitudinal **hole** (22) through it for a strip electrode (23). Two flat **capacitors** (24,25) are **mounted** on the **top surface**, end to end, with end electrodes (24c,d; 25c,d). The two projecting ends (23a,b) are bent upwards and over to make contact with the outer electrodes (24c,25c) of the two capacitors.

The other two inner electrodes (24d,25d) are connected by a spanning element (28) formed by another strip electrode bent into an inverted U shape which also forms a clamp. In another design, the two capacitors fit into a sunken zone on top.

ADVANTAGE - The design is simpler than existing filters.

.5/18

Abstract (Equivalent): DE 3432670 C

The noise suppressing filter (20) has a main block (21) of ferro-magnetic material and this has a rectangular section slot (22) through which a strip shaped electrode passes (23). The top ends of the strip are turned through 90 deg. (26,27) to contact the ends of a pair of capacitor elements (24,25).

The electrical capacitors are formed with dielectric layers (24b,25b) into which internal electrodes (24a,25a) are embedded. The ends of the capacitors have contact elements (24c,25c) with the inner ends coupled by a common contact (28). (8pp)

Abstract (Equivalent): US 4571561 A

The filter comprises a block of magnetisable material, and two laminated capacitors each having two terminal electrodes opposite to each other. The **capacitors** are **mounted** on one **surface** of the block with the second terminal electrodes of the respective capacitors spacedly confronting each other. The filter also comprises a first electrode member partially extending through the block with its opposite end portions connected to the first terminal electrodes of the

respective capacitors.

A second electrode member is mounted on the block with a portion **electrically connecting** the second terminal electrodes of the respective capacitors together.

ADVANTAGE - Requires no time-consuming processes. (9pp)

22/3,AB/12 (Item 12 from file: 350)  
DIALOG(R)File 350:Derwent.WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

004067850

WPI Acc No: 1984-213391/198434

XRAM Acc No: C84-089640

XRPX Acc No: N84-159756

Aluminium electrolysis process - uses crust breaking tool controlled by impedance measuring circuit

Patent Assignee: HEINZMANN U (HEIN-I); SCHWEIZ ALUMINIUM AG (SWAL )

Number of Countries: 014 Number of Patents: 010

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8403108	A	19840816	WO 84CH19	A	19840209	198434 B
DE 3305236	A	19840920	DE 3305236	A	19830216	198439
AU 8424373	A	19840830				198446
NO 8404033	A	19841227				198507
EP 135516	A	19850403	EP 84900604	A	19840209	198514
DE 3305236	C	19851121				198548
US 4563255	A	19860107	US 84667488	A	19841001	198605
EP 135516	B	19861015				198642
DE 3460987	G	19861127				198649
IT 1175323	B	19870701				199029

Priority Applications (No Type Date): CH 83739 A 19830210

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
-----------	------	-----	----	----------	--------------

WO 8403108	A	G			
------------	---	---	--	--	--

Designated States (National): AU NO US

Designated States (Regional): AT BE CH DE FR GB LU NL SE

EP 135516	A	G			
-----------	---	---	--	--	--

Designated States (Regional): AT BE CH DE FR GB LI LU NL SE

EP 135516	B	G			
-----------	---	---	--	--	--

Designated States (Regional): AT CH DE FR GB LI NL SE

Abstract (Basic): EP 135516 A

Method for controlling a knock-in device with up/downwardly moving chisel (30) for the crust forming on the molten electrolyte (14) of a fusion electrolysis cell, by detection of the contacting of chisel/molten electrolyte, where signal variations effected by variations of the impedance between chisel and molten electrolyte are detected for control with the chisel (30) as measuring sensor in an electric measuring circuit, characterised in that the impedance between chisel (30) and molten electrolyte (14) is detected by means of an active impedance-measuring circuit (38,40,32,34).

(10pp)

DE 3305236 A

During the production of Al by electrolysis a **surface** crust is for formed on top of the molten electrolyte bath. To maintain an **opening** in the crust for feeding alumina into the bath an air powered tool operates a punching chisel to break the crust. The tool is regulated by a control loop comprising an active signal source and an impedance measuring circuit. The impedance

measurements and control circuitry provides precise regulation of the chisel.

In the idle position the chisel is raised clear of the bath and crust. In operation downward pressure is exerted on the chisel to contact the crust. Resistance to breakthrough is signalled through the control circuit to provide additional power to the chisel. After the chisel has broken through the crust and is in contact with the molten electrolyte the transmitted signal actuates the control system to return the chisel to the upper ideal position. The control circuitry is protected from the effects of the anode and cathode voltages and stray currents by means of capacitors in the circuit.

USE/ADVANTAGE - The power to operate the chisel is fully controlled thus avoiding any waste of excess energy. The chisel is raised clear of the bath when in the idle position thus avoiding the effects of corrosion and temperature. The control system will indicate any defects in the air supply or in the electrical insulation of the tool and anodes.

(14pp

Abstract (Equivalent): EP 135516 B

Method for controlling a knock-in device with up/downwardly moving chisel (30) for the crust forming on the molten electrolyte (14) of a fusion electrolysis cell, by detection of the contacting of chisel/molten electrolyte, where signal variations effected by variations of the impedance between chisel and molten electrolyte are detected for control with the chisel (30) as measuring sensor in an electric measuring circuit, characterised in that the impedance between chisel (30) and molten electrolyte (14) is detected by means of an active impedance-measuring circuit (38,40,32,34).

Abstract (Equivalent): WO 8403108 A

During the production of Al by electrolysis a **surface** crust is formed on top of the molten electrolyte bath. To maintain an **opening** in the crust for feeding alumina into the bath an air powered tool operates a punching chisel to break the crust. The tool is regulated by a control loop comprising an active signal source and an impedance measuring circuit. The impedance measurements and control circuitry provides precise regulation of the chisel.

In the idle position the chisel is raised clear of the bath and crust. In operation downward pressure is exerted on the chisel to contact the crust. Resistance to breakthrough is signalled through the control circuit to provide additional power to the chisel. After the chisel has broken through the crust and is in contact with the molten electrolyte the transmitted signal actuates the control system to return the chisel to the upper idle position. The control circuitry is protected from the effects of the anode and cathode voltages and stray currents by means of capacitors in the circuit.

USE/ADVANTAGE - The power to operate the chisel is fully controlled thus avoiding any waste of excess energy. The chisel is raised clear of the bath when in the idle position thus avoiding the effects of corrosion and temperature. The control system will indicate any defects in the air supply or in the electrical insulation of the tool and anodes.

0/2

US 4563255 A

Crust breaker (28) for a fused salt electrolytic cell, partic. for Al production is controlled by an **electrical** circuit which **connects** the **top surface** of the breaker to a point (38) on the steel pot at cathode potential and is fed by an alternating current from a source (32) providing an AC voltage of e.g. 24V. An electronic relay (34) measures a resultant AC signal which is a function of circuit impedance and emits a corresp. signal to the process control **unit** (36). Two neutralising **capacitors** (40) effect separation of the DC potential between the electrolytic cell and

the process control or relay (34).

ADVANTAGE - Penetration of the crust is ensured by control of energy supplied to the breaker, the reliability of which is increased.

(7pp

22/3,AB/13 (Item 13 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

003270966

WPI Acc No: 1982-B8949E/198208

Laminated ceramic chip carrier has high internal capacitors - arranged to match thermal expansion of chip and carrier

Patent Assignee: IBM CORP (IBM )

Inventor: BAJOREK C H; CHANCE D A; HO C W

Number of Countries: 006 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 45877	A	19820217	EP 81105736	A	19810721	198208 B
JP 57037818	A	19820302				198214
US 4349862	A	19820914				198239
EP 45877	B	19841031				198444
DE 3166953	G	19841206				198450

Priority Applications (No Type Date): US 80176949 A 19800811

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
-----------	------	-----	----	----------	--------------

EP 45877	A	E	26		
----------	---	---	----	--	--

Designated States (Regional): DE FR GB IT

EP 45877	B	E			
----------	---	---	--	--	--

Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 45877 A

The laminated sheet printed circuit carrier (1) includes capacitors (9) formed from **disc**-shaped bits of material, hinging a much higher dielectric constant than the ceramic material, and associated conductive portions. The matrix of dielectric **discs** is so arranged that the thermal coefficient of expansion of the carrier matches that of silicon integrated circuit chips (11) with which it will be used. The capacitors may be formed by filling **holes** in one lamination (2) with the dielectric material and forming the conductive portions on the upper and **lower surfaces** of the laminations. Alternatively, the **holes** may be filled with conductive material and the dielectric **discs** aligned with the **holes** in the lamination.

Alternatively the capacitors could be provided in a void between two laminations and **electrically connected** to printed circuits on them. The carrier prevents the build up of stress in solder ball joints between itself and the chip (11) due to differential thermal expansion yet has high capacitance. The device is also used for **mounting discrete capacitors** or chip carriers.

1

22/3,AB/14 (Item 1 from file: 347)  
DIALOG(R)File 347:JAPIO  
(c) 2004 JPO & JAPIO. All rts. reserv.

04334374

CONNECTOR WITH BUILT-IN COAXIAL CAPACITOR

PUB. NO.: 05-326074 [JP 5326074 A]  
PUBLISHED: December 10, 1993 (19931210)  
INVENTOR(s): IRIE SHOICHI  
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company  
or Corporation), JP (Japan)  
APPL. NO.: 04-124403 [JP 92124403]  
FILED: May 18, 1992 (19920518)  
JOURNAL: Section: E, Section Number 1519, Volume 18, Number 139, Pg. 103,  
March 08, 1994 (19940308)

#### ABSTRACT

PURPOSE: To facilitate replacing of a coaxial capacitor for removing an unnecessary high frequency component by internally providing a movable plate to push up the coaxial capacitor outside.

CONSTITUTION: Coaxial capacitors 1 are set to **holes** of a connector body 4 by using pins 2 **electrically connected** to electrodes 5. A protrusion part 6 is provided in the inside of the body 4, to further provide a movable plate 3, provided with escaping **holes** in the vicinity of a central part so that the pins 2 can be inserted, in the body 4. The capacitor is fitted to the **hole** of the body 4, to further fit the pin 2 to a **hole** of the capacitor 1 inserted, and by the movable plate 3 provided with the escape **hole** in the vicinity of the central part so that the pin 2 can be inserted through a **bottom surface** of the **mounted capacitor** 1, it is lifted. In this way, a several number of the capacitors 1 can be simultaneously removed from the body 4.

22/3,AB/15 (Item 2 from file: 347)  
DIALOG(R)File 347:JAPIO  
(c) 2004 JPO & JAPIO. All rts. reserv.

02324516  
CRYSTAL RESONATOR

PUB. NO.: 62-241416 [JP 62241416 A]  
PUBLISHED: October 22, 1987 (19871022)  
INVENTOR(s): YOSHIDA YUKIO  
TANAKA ATSUSHI  
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company  
or Corporation), JP (Japan)  
APPL. NO.: 61-085361 [JP 8685361]  
FILED: April 14, 1986 (19860414)  
JOURNAL: Section: E, Section Number 598, Volume 12, Number 111, Pg. 109, April  
08, 1988 (19880408)

#### ABSTRACT

PURPOSE: To package electronic parts to high density by holding a plate type capacitor obtained by forming two capacitors on the **top surface** of a glass part in one body by using an airtight terminal, holding a crystal element almost at right angles to the main **surface** of the capacitor, and also pressing a metallic cap onto the airtight terminal.

CONSTITUTION: Inner leads 7 and 7' of the airtight terminal 19 are inserted into through **holes** 31 and 31' of the **capacitor** 30 and **mounted** on the **top surface** of the glass part 12 of the airtight terminal, and the tip part of a lead wire 11 and the electrode 8

of the capacitor 30 are held mechanically and **connected electrically**. Then, the almost rectangular crystal element 1 is mounted almost at right angles to the main **surface** of the capacitor 30 and held mechanically by using, for example, solder materials 4 and 4'. Then, while the crystal element 1 is oscillated through lead wires 10, 10', and 11, metal is stuck on an exciting electrode 2 by vapor deposition, etc., to adjust an oscillation frequency. Then, the metallic cap 14 is pressed onto the airtight terminal 19 to seal the capacitor 30 and crystal element 1 airtightly.

24/3,AB/1 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

013058137

WPI Acc No: 2000-230005/200020

XRPX Acc No: N00-173212

**Stack** type **capacitor** structure for dynamic random access  
memory or ferroelectric RAM

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000049302	A	20000218	JP 98216269	A	1998073	200020	B

Priority Applications (No Type Date): JP 98216269 A 19980730

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000049302	A		27	H01L-027/108	

Abstract (Basic): JP 2000049302 A

Abstract (Basic):

NOVELTY - A thin polysilicon (15) is **electrically connected** to the source or drain side of a transistor formed on a silicon **substrate** (1) through an embedded polysilicon (13). The embedded polysilicon is formed on the **aperture** circles of intermediate insulating films (7,9). A part of the embedded polysilicon is formed protruding from an insulating film (9), and used as the capacitor lower electrode.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the DRAM or FRAM manufacture.

USE - For DRAM or FRAM.

ADVANTAGE - Reduces absolute steps on cell **portion** and **peripheral portion** to obtain identical capacitance. Uses simple photolithography and etching process when performing wiring on the top layer of the DRAM or FRAM. Has miniaturized structure and high integration.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view showing the components of the DRAM.

Silicon **substrate** (1)

Insulating films (7,9)

Embedded polysilicon (13)

Thin polysilicon (15)

pp; 27 DwgNo 2/46

26/3,AB/1 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

(c) 2004 JPO & JAPIO. All rts. reserv.

02597036

MANUFACTURE OF HYBRID INTEGRATED CIRCUIT DEVICE

PUB. NO.: 63-213936 [JP 63213936 A]

PUBLISHED: September 06, 1988 (19880906)

INVENTOR(s): YANAGISAWA KATSUAKI

APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP  
(Japan)

APPL. NO.: 62-048020 [JP 8748020]

FILED: March 02, 1987 (19870302)

JOURNAL: Section: E, Section Number 700, Volume 13, Number 2, Pg. 76, January  
06, 1989 (19890106)

#### ABSTRACT

PURPOSE: To enable electronic components to be bonded reliably with solder to both sides of a printed circuit board, by including a step for filling through **holes** with solder paste simultaneously with applying the solder paste on electronic component carrying lands.

CONSTITUTION: A **semiconductor die** bonding land 2 and an electronic component carrying land 3 are formed on one face of a double-side printed circuit board with through **holes** provided in an alumina **substrate** 1. Solder paste is supplied not only to these lands 2 and 3 but also to the through **holes** 5 so that the through **holes** 5 are filled with the solder paste 4. After that, a semiconductor pellet 6 and a chip **capacitor** 7 are **mounted** and bonded by reflowing the solder. The semiconductor pellet 6 is then **electrically connected** to the double-side circuit board by bonding Au wires 10 and covered with silicon resin 8. Subsequently, a chip capacitor 9 is bonded to the opposite side of the double-side printed circuit board by means of molten solder. Thus, the silicon resin for protecting the semiconductor pellet penetrates into the through **holes** and does not inhibit electronic components from being bonded with solder. Accordingly, a hybrid integrated circuit having a high reliability can be obtained.

28/3,AB/1 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015872648

WPI Acc No: 2004-030479/200403

XRPX Acc No: N04-023952

Printed circuit board for analog and digital electronic systems, has capacitor whose one terminal is directly attached to power plane and other terminal is indirectly connected to ground plane

Patent Assignee: SUN MICROSYSTEMS INC (SUNM )

Inventor: NOVAK I; ST CYR V

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6608257	B1	20030819	US 200121769	A	20011212	200403 B

Priority Applications (No Type Date): US 200121769 A 20011212

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6608257	B1	12	H05K-001/02		

Abstract (Basic): US 6608257 B1

Abstract (Basic):

NOVELTY - The printed circuit board (20) consists of a power plane (40) arranged between an outermost signal layer (25) and a ground plane (50). A **capacitor** (35) **mounted** within a cavity (30), extending from the signal layer to the power plane, has its one terminal (38) directly attached to power plane and other terminal (39) **electrically connected** to the ground plane through an **opening** in the power plane.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for capacitor attachment method on printed circuit board.

USE - Printed circuit board (PCB) **mounted** with thin-film **capacitor, surface mounted capacitor, ball-grid array (BGA) capacitor** or multi-terminal capacitor, for analog and digital electronic systems.

ADVANTAGE - Due to the attachment of one capacitor terminal directly to power plane, the current path between power and ground planes is made shorter and thereby the impedance in the electronic system is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows the side view of the capacitor attached to printed circuit board.

printed circuit board (20)  
outermost signal layer (25)  
cavity (30)  
capacitor (35)  
capacitor terminals (38,39)  
power plane (40)  
ground plane (50)  
pp; 12 DwgNo 6B/6

28/3,AB/2 (Item 2 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

013196830

WPI Acc No: 2000-368703/200032

XRPX Acc No: N00-276022

Socket board used for mounting integrated circuit during test,  
**mounts** chip **capacitor** vertically on undersurface and  
**electrically connects** capacitor terminals with that of  
semiconductor device via through-**holes**

Patent Assignee: ANDO ELECTRIC CO LTD (ANDN )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11312766	A	19991109	JP 98119587	A	19980428	200032 B

Priority Applications (No Type Date): JP 98119587 A 19980428

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11312766	A	5	H01L-023/32	

Abstract (Basic): JP 11312766 A

Abstract (Basic):

NOVELTY - Socket board (21) mounts semiconductor device (11) on the upper **surface**, vertically **mounts** the chip **capacitor** (7) on the under **surface** and has through-**holes** (6) connecting the terminals of the semiconductor device with the terminals of the chip capacitor.

USE - For mounting semiconductor IC such as **BGA** package during test.

ADVANTAGE - Enables to directly attach the chip component to arbitrary pins and to reduce the installation area of the chip component on the back side of the socket board. Eliminates the problem of covering the through-**holes** with the chip component and enables to reliably mount the chip component. Prevents damage of the chip capacitor by contacting with other components.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic sectional view of the socket board.

Through-**holes** (6)

Chip capacitor (7)

Semiconductor device (11)

Socket board (21)

pp; 5 DwgNo 1/9

33/3,AB/1 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015862550

WPI Acc No: 2004-020381/200402

XRAM Acc No: C04-006243

XRPX Acc No: N04-015685

Inductor-capacitor type filter module for helical filter has at least two capacitors, each having first elongated element and second element both made of conductive material, and inductors(s) with coil that is carried by support body

Patent Assignee: BRUKER BIOSPIN SA (BRUK-N)

Inventor: BREVARD C; GONELLA O; WEISS M

Number of Countries: 032 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030137369	A1	20030724	US 2003348898	A	20030123	200402 B
EP 1331733	A1	20030730	EP 2002360375	A	20021220	200402
FR 2835092	A1	20030725	FR 2002831	A	20020123	200402
JP 2003249833	A	20030905	JP 200313473	A	20030122	200402

Priority Applications (No Type Date): FR 2002831 A 20020123

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
-----------	------	-----	----	----------	--------------

US 20030137369	A1		9	H01P-001/20	
----------------	----	--	---	-------------	--

EP 1331733	A1	F		H03H-003/00	
------------	----	---	--	-------------	--

Designated States (Regional): AL AT BE BG CH CY CZ DE DK EE ES FI FR GB

GR IE IT LI LT LU LV MC MK NL PT RO SE SI SK TR

FR 2835092	A1			H01G-017/00	
------------	----	--	--	-------------	--

JP 2003249833	A		7	H03H-007/075	
---------------	---	--	---	--------------	--

Abstract (Basic): US 20030137369 A1

Abstract (Basic):

NOVELTY - An inductor-capacitor (L-C) type filter module comprises:

(a) at least 2 capacitors having elongated element made of a conductive material (I) partially fitted over a determined depth in a **hole** or perforation of a second element (II) also made of (I);  
and

(b) inductors(s) having a coil carried by a support body contiguous with (II) or a dielectric coating covering an external face of each (II)

DETAILED DESCRIPTION - An L-C type filter module comprises at least two capacitors (2, 2') and inductors(s). Each capacitor comprises a first elongated element (4, 4') made of a conductive material partially fitted, over a determined depth, in a **hole** or perforation (5) of a second element (6) made of the conductive material **connected electrically** to the second elements of the other capacitors or possibly common to the various capacitors. The internal lateral **surface** defining the **holes** or perforations are covered with a dielectric material (7), as are the edges (5') of the **openings** of the **holes** or perforations and the external **surfaces** of the second elements adjoining the edges. A coil (3') of each inductor (3) is carried by a support body (8) made of the dielectric material, contiguous with the second element(s) or with the dielectric coating at least partially covering an external face of each second element.

An INDEPENDENT CLAIM is included for a helical filter at least of the order 2 with a module structure. The helical filter is formed by the series connection of at least two filter modules. Each module has specific filtering characteristics that can be adjusted by regulating

the characteristics of the capacitor. Each various module is housed in a corresponding closed compartments of a box forming a Faraday cage, while being electromagnetically insulated from the exterior of the module(s) forming the filter.

USE - The inductor-capacitor (L-C) type filter module is used as a helical filter (claimed).

ADVANTAGE - The module is easy to manufacture and assemble in variable numbers, with a low manufacturing cost and very good filtering properties. It obtains improved voltage resistance, very good protection of the capacitors against the risk of arcing (between the first and second elements), and, if necessary, a very compact structure.

DESCRIPTION OF DRAWING(S) - The figure shows a section of a filter module.

Common electric node (1')

Capacitors (2, 2')

Inductor (3)

Coil (3')

First elongated element (4, 4')

Hole or perforation (5)

Edges (5')

Second element (6)

Dielectric material (7)

Support body (8)

Branch terminals (9, 9')

Connection line (14)

pp; 9 DwgNo 1/4

33/3,AB/2 (Item 2 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015806721

WPI Acc No: 2003-868925/200381

XRPX Acc No: N03-693621

Electrical component housing for outdoor unit of air conditioner, has **base with opening for connecting electrical**

component of housing with electrical component of machine room

Patent Assignee: DAIKIN KOGYO KK (DAIK )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2003240277	A	20030827	JP 200241146	A	20020219	200381 B

Priority Applications (No Type Date): JP 200241146 A 20020219

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2003240277	A	8	F24F-005/00	

Abstract (Basic): JP 2003240277 A

Abstract (Basic):

NOVELTY - The housing main portion (53) having a **base** (534) with an **opening**, is arranged facing a machine room. An electric component (52) of the housing is connected to the electric component of the machine room, through the **base opening**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for outdoor unit.

USE - For accommodating electrical components such as power transistor and **capacitor** in outdoor **unit** (claimed) of air

conditioner.

ADVANTAGE - The housing is attached to the outdoor unit easily, thereby improving the assembling property of outdoor unit.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective view of electrical component housing.

electrical component housing (50)

electrical component (52)

housing main portion (53)

cover (55)

connector (522)

**base** (534)

pp; 8 DwgNo 5/7

33/3,AB/3 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent, All rts. reserv.

015643294

WPI Acc No: 2003-705477/200367

Power amplifier of mobile communication instrument

Patent Assignee: SAMSUNG ELECTRO MECHANICS CO LTD (SMSU )

Inventor: PARK T J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
KR 2003043061	A	20030602	KR 200174021	A	20011126	200367 B

Priority Applications (No Type Date): KR 200174021 A 20011126

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2003043061	A		1	H04B-001/44	

Abstract (Basic): KR 2003043061 A

Abstract (Basic):

NOVELTY - A power amplifier of a mobile communication device is provided to accumulate high permittivity ceramic layers and low permittivity ceramic layers by using an LTCC (Low Temperature Co-Fired Ceramic) **substrate**, and to print capacitor components on the high permittivity ceramic layers and inductor components on the low permittivity ceramic layers.

DETAILED DESCRIPTION - The first **substrate** (41) is composed of many accumulated high permittivity layers. The second **substrate** (42) is composed of many low permittivity layers accumulated on the first **substrate**. An interstage matching circuit forming unit (43) is made up from many capacitance patterns, formed on the first **substrate**. An inductance pattern (P2) is **electrically connected** to one end of the capacitance patterns through a via **hole**, and is formed on many low permittivity layers. A bypass capacitor (P3) is connected to one end of the inductor pattern, and is printed crosswise on a layer between the capacitance patterns. A bypass **capacitor** forming unit (44) comprises bypass capacitance pattern (P6) printed on the layers of the first **substrate**. One end of the bypass capacitance patterns is connected to a ground pattern (P5) by the via **hole**, and the other end is connected to a power amplifier.

pp; 1 DwgNo 1/10

33/3,AB/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015170678

WPI Acc No: 2003-231206/200323

XRPX Acc No: N03-183908

Electronic unit for vehicle, has one pin pressed into **aperture** in first conducting **surface** of first polarity, another pressed into second **surface** of second polarity, and insulating layer between **surfaces**

Patent Assignee: CONTI TEMIC MICROELECTRONIC GMBH (TELE )

Inventor: GEORGE D; GREIF A; SCHIRMER E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 10121108	A1	20021128	DE 1021108	A	20010428	200323 B

Priority Applications (No.Type Date): DE 1021108 A 20010428

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10121108	A1		4	H01G-004/38	

Abstract (Basic): DE 10121108 A1

Abstract (Basic):

NOVELTY - The electronic **unit** has a **capacitor unit** (1) with several **capacitors** (5) with press-in pin connectors (6). One pin is pressed into an **aperture** in a first conducting **surface** (2) of a first polarity and another is pressed into a second conducting **surface** (3) of a second polarity and separated from the first conducting **surface** by an insulating layer (4).

USE - Especially for control and/or regulation of specific vehicle processes.

ADVANTAGE - Simple design, simple manufacture, low costs, high reliability and advantageous properties in relation to **electrical connections**.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic representation of a section of an inventive **capacitor unit**

**Capacitor unit** (1)

Capacitors (5)

Connectors (6)

First and second conducting **surfaces** (2,3)

Insulating layer (4)

pp; 4 DwgNo 1/4

33/3,AB/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

014805840

WPI Acc No: 2002-626546/200267

XRAM Acc No: C02-176599

XRPX Acc No: N02-495479

Manufacture of displaying unit for flat display **panel** involves patterning and etching first conduction layer, active layer, second conduction layer, third and second isolation layers, and fourth conduction layer

Patent Assignee: IND TECHNOLOGY RES INST (INTE-N); CHEN C (CHEN-I); TAI Y (TAIY-I)

Inventor: CHEN J; DAI Y; CHEN C; TAI Y  
Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020081761	A1	20020627	US 2001848257	A	20010504	200267 B
US 6432734	B1	20020813	US 2001848257	A	20010504	200267
TW 471181	A	20020101	TW 2000128028	A	20001227	200281

Priority Applications (No Type Date): TW 2000128028 A 20001227

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020081761	A1	14		H01L-021/00	
US 6432734	B1			H01L-029/00	
TW 471181	A			H01L-029/786	

Abstract (Basic): US 20020081761 A1

Abstract (Basic):

NOVELTY - A displaying unit is manufactured by patterning and etching first conduction layer, active layer, second conduction layer, third and second isolation layers, and fourth conduction layer, on a **substrate** (300). The patterning and etching of the second conduction layer form components to constitute a storage **capacitor** of the displaying unit.

DETAILED DESCRIPTION - Manufacture of a displaying unit comprises forming a first conduction layer on a **substrate**. The first conduction layer is patterned and etched to form gate layer (301) and bottom electrode layer on the **substrate**. A first isolation layer (303) and an active layer are sequentially formed on the **substrate**. The active layer is patterned and etched to form an island-like layer over the gate layer. A second conduction layer is formed over the **substrate**. The second conduction layer is patterned and etched to form two source/drain electrodes, top electrode (307) layer, and common contact layer (308). The source/drain electrodes overlap the two portions of the island-like layer (304). The bottom electrode layer, first isolation layer, and top electrode layer constitute a storage **capacitor** of the displaying unit. A second isolation layer (309) and a third conduction layer are subsequently formed on the **substrate**. The third and second isolation layers are patterned and etched to form at least five contact **holes** (OP1-OP5). The first source/drain electrode (305, 306) is revealed in the first contact **hole**, a common electrode layer (310) is revealed in the second and third contact **holes**, the top electrode layer is revealed in the fourth contact **hole**, and common contact layer is revealed in the fifth contact **hole**. A fourth conduction layer is formed on the third isolation layer (311), then filled into the first to fifth contact **holes**. The fourth conduction layer is patterned and etched to form pixel electrodes, and two connecting layers on the third isolation layer. The first source/drain electrode in the first contact **hole** and common electrode layer in the second contact **hole** are **electrically connected** via the first connecting layer. The common electrode layer in the third contact **hole** is **electrically connected** via the second connecting layer. The pixel electrodes are **electrically connected** to the second contact layer through the first contact **hole**.

USE - For manufacturing a displaying unit or pixel unit for flat display **panel**.

ADVANTAGE - The inventive method provides a flat display with wide viewing angle. It reduces the number of masks from seven to six in fabricating a pixel unit, as well as fabrication costs.

DESCRIPTION OF DRAWING(S) - The drawing shows a step of the inventive fabricating process of the pixel unit of the liquid crystal display panel.

Substrate (300)  
Gate layer (301)  
First isolation layer (303)  
Island-like layer (304)  
Source/drain electrode (305, 306)  
Top electrode (307)  
Common contact layer (308)  
Second isolation layer (309)  
Common electrode layer (310)  
Third isolation layer (311)  
Five contact **holes** (OP1-OP5)  
pp; 14 DwgNo 3E/3

33/3,AB/6 (Item 6 from file: 350)  
DIALOG(R)File 350;Derwent.WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

014373680

WPI Acc No: 2002-194383/200225

XRAM Acc No: C02-060021

XRPX Acc No: N02-147567

Dynamic random access memory fabrication includes two stages of contact plug formation

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)

Inventor: JIANG M; JIANG W; WU J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
TW 421887	A	20010211	TW 99107970	A	19990517	200225 B

Priority Applications (No Type Date): TW 99107970 A 19990517

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
TW 421887	A	31	H01L-027/108	

Abstract (Basic): TW 421887 A

Abstract (Basic):

NOVELTY - After **capacitor** formation on memory unit region, etching stop layer formed on capacitor **surface** is used as blocking mask to form first stage contact plug **electrically connected** with word line. Insulating layer is then formed on whole **surface**. Second stage contact plug which punches through insulating layer and **electrically connects** with first stage contact plug is then formed.

USE - Dynamic random access memory fabrication.

ADVANTAGE - Conventional problems such as insufficient optical resolution and an over-large aspect ratio of contact **hole** can be solved, while avoiding capacitor damage.

pp; 31 DwgNo 1A/2

33/3,AB/7 (Item 7 from file: 350)  
DIALOG(R)File 350;Derwent.WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

012678552

WPI Acc No: 1999-484659/199941

XRAM Acc No: C99-142495

XRPX Acc No: N99-361688

Solid state electrolytic capacitor for various electronic machines - has external positive terminal filled with one end of outer cladding case, and connected to conductive material through conductive material connection layer

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11204376	A	19990730	JP 987268	A	19980119	199941 B

Priority Applications (No Type Date): JP 987268 A 19980119

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 11204376	A	9	H01G-009/004	

Abstract (Basic): JP 11204376 A

NOVELTY - An external positive terminal (20) is fitted with one end of an outer cladding case (18). The external positive terminal is **connected electrically** with a metal conductive material (15) through a conductive material connection layer (14).

DETAILED DESCRIPTION - A capacitor (11) has a dielectric oxide film, a solid electrolyte layer and a catholyte (16) on the **surface** of an anode body. An anode derivation line (12) is provided under the anode body. A conductive material connection layer (17) connects the catholyte of the **capacitor unit** with the external cathode terminal. The external cathode terminal (19) gets fitted with the other end of the outer cladding case. An insulation layer (13) buries a **gap** between the outer cladding case and the anode derivation **surface** of the anode body. The metal conductive material is connected with the anode derivation line. The solid electrolyte layer provided by the **capacitor unit** is made from a conductive polymer.

An INDEPENDENT CLAIM is also included for manufacture of the electrolytic capacitor.

POLYMERS - The solid electrolyte layer of the capacitor is made from a conductive polymer.

USE - For various electronic machines.

ADVANTAGE - Has stable resistance characteristics thereby improving dimensional accuracy and increasing the productivity of electronic machine. Capacity is increased, since the space between external positive terminal and external cathode terminal is reduced.

DESCRIPTION OF DRAWING - The figure is a perspective view of outer cladding case in which external cathode terminal is fitted. (11) Capacitor; (12) Anode derivation line; (13) Insulation layer; (14,17) Conductive material connection layers; (15) Metal conductive material; (16) Catholyte; (18) Outer cladding case; (19) External cathode terminal; (20) External positive terminal.

Dwg.12/19

33/3,AB/8 (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

011482429

WPI Acc No: 1997-460334/199743

XRPX Acc No: N97-383289

Integrated electro-optical unit for portable electronic equipment - has optically-transparent **substrate** which has central row and column positioned LEDs with integrated ring support and **electrical connections**

Patent Assignee: MOTOROLA INC (MOTI )

Inventor: LEBBY M S; RICHARD F V; STAFFORD J W

Number of Countries: 005 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
FR 2745676	A1	19970905	FR 972480	A	19970303	199743 B
JP 9244552	A	19970919	JP 9763941	A	19970304	199748
US 5699073	A	19971216	US 96610501	A	19960304	199805
KR 97067057	A	19971013	KR 976195	A	19970227	199842
TW 382799	A	20000221	TW 97100796	A	19970124	200050

Priority Applications (No Type Date): US 96610501 A 19960304

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2745676	A1	36	H04N-005/30		
JP 9244552	A	15	G09F-009/33		
US 5699073	A	19	G09G-003/32		
KR 97067057	A		G09F-009/35		
TW 382799	A		H01L-027/00		

Abstract (Basic): FR 2745676 A

The unit has an outer moulded housing (50) which contains integrated electrical supplies (51'). A control card (30) contains a central **opening** (33). An optical transmitter (14) is positioned below the central **opening**, which has an upper lens unit (60). The transmitter is formed from controllable rows and columns of LEDs.

The control **unit** section has **capacitors** and integrated components and commands are passed via through **hole** connections (44) and wire connections (36) to connection pads on the optical **surface**.

USE/ADVANTAGE - E.g. cellular and cordless telephones, pager, databank applications. Allows optical display to be constructed with small height and low power consumption.

Dwg.6/19

Abstract (Equivalent): US 5699073 A

The unit has an outer moulded housing (50) which contains integrated electrical supplies (51'). A control card (30) contains a central **opening** (33). An optical transmitter (14) is positioned below the central **opening**, which has an upper lens unit (60). The transmitter is formed from controllable rows and columns of LEDs.

The control **unit** section has **capacitors** and integrated components and commands are passed via through **hole** connections (44) and wire connections (36) to connection pads on the optical **surface**.

USE/ADVANTAGE - E.g. cellular and cordless telephones, pager, databank applications. Allows optical display to be constructed with small height and low power consumption.

Dwg.4/19

33/3,AB/9 (Item 9 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

010137904

WPI Acc No: 1995-039155/199506

XRPX Acc No: N95-031029

Static electricity protection wrist strap used in mfr. of computer and communication equipment -- has processing unit provided with bleeper which sends out warning signal when increase is detected of electricity collected on skin

Patent Assignee: YANG H (YANG-I)

Inventor: YANG H

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
GB 2279875	A	19950118	GB 9320199	A	19930930	199506 B
US 5457596	A	19951010	US 9382203	A	19930624	199546
GB 2279875	B	19970305	GB 9320199	A	19930930	199713

Priority Applications (No Type Date): US 9382203 A 19930624

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2279875	A		17	A61N-001/14	
US 5457596	A		8	H05F-003/02	
GB 2279875	B			A61N-001/14	

Abstract (Basic): GB 2279875 A

The strap has an insulating casing (90) inside which a conductive plate (3) is mounted. The plate has serrated side extensions for engaging a strap (4) extending from one side of the casing, around the wrist of a user and back to the other side of the casing. A wire in connection with the plate through a plug (12) provides the strap with a grounding connection.

A static electricity detection device includes a plate on the underside of a circuit board (5) which constitutes a capacitor with the skin (62) of the wrist wearing the strap. A processing unit includes a beeper which sends out a warning signal when an increase of the static electricity collected on the skin is detected, indicating failure of the ground connection.

ADVANTAGE - Provides indication of damage of grounding wire, so preventing unexpected static electricity accident.

Dwg.3/5

Abstract (Equivalent): GB 2279875 B

A static electricity protection wrist strap comprising: a casing having an electrical insulation cover member tightly engaging an electrical insulation **base** member to define therein an interior space; a conductive plate disposed inside the interior space to be substantially received within the cover member, the conductive plate comprising two opposite side extensions each having a sharp serration structure formed thereon; a strap member having conductive filaments contained therein extending from one of the serrated side extensions of the conductive plate, through a side **opening** formed on the casing to outside the casing to surround a wrist of a user and returning through a second side **opening** of the casing to connect to the other one of the serrated side extensions, the serrations penetrating the strap member to electrically contact the conductive filaments inside the strap member; a conductive plug extending through a **hole** formed on the cover member and a corresponding **hole** formed on the conductive plate to project out of the casing and secured thereto by a fastener; a conductive wire connected between the conductive plug and ground; a static electricity detection device comprising a circuit board disposed inside the interior space and below the conductive plate to oppose the **base** member, the circuit board being in **electrical connection** with the conductive plate and having a detection plate mounted on an underside thereof to face a...

corresponding bottom **opening** formed on the **base** member so as to allow the detection plate and skin of the wrist to form a capacitor structure of which the charge is to be detected, the circuit board comprising an actuation switch for actuating the static electricity detection device; and a warning device which sends out a warning signal once the detected charge exceeds a pre-set level.

Dwg.1

Abstract (Equivalent): US 5457596 A

A static electricity protection wrist strap comprises a casing inside which a conductive plate is mounted. The conductive plate has serrated side extensions for engaging a strap extending from one side of the casing, around the wrist of a user and back to connect to the other side of the casing. A grounding wire in **electrical connection** with the conductive plate provides the static electricity protection wrist strap a grounding connection. A static electricity detection device comprises a detection plate which constitutes a capacitor with the skin of the wrist wearing the wrist strap and a processing unit for detecting the variation of the **capacitor**. The processing **unit** comprises a beeper which will be actuated to send out a warning signal when an increase of the static electricity collected on the wrist skin is detected.

Dwg.3/5

33/3,AB/10 (Item 10 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

009850556

WPI Acc No: 1994-130412/199416

XRPX Acc No: N94-102601

Dielectric filter having pair of resonators in parallel with electromagnetic coupling - holds polarising capacitor to lead terminal and **electrically connected** by holder **unit** at terminal, where **capacitor** is formed by **gap** and dielectric **substrate** is formed by electrode pair interleaving **gap**

Patent Assignee: KYOCERA CORP (KYOC )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 6077706	A	19940318	JP 92230183	A	19920828	199416 B

Priority Applications (No Type Date): JP 92230183 A 19920828

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6077706	A		4	H01P-001/205	

Abstract (Basic): JP 6077706 A

Dwg.1,2/5

33/3,AB/11 (Item 11 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

009512549

WPI Acc No: 1993-206085/199326

XRPX Acc No: N93-158508

Vehicle electronic control unit after-running controller - has resistor-capacitor T-network between ignition switch and control

unit with **capacitor discharging** after ignition  
switch-off maintaining voltage to ECU for short time  
Patent Assignee: BOSCH GMBH ROBERT (BOSC )  
Inventor: ARNOLD H; GANTENBEIN R  
Number of Countries: 004 Number of Patents: 005  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DE 4141586	A1	19930624	DE 4141586	A	19911217	199326 B
FR 2685142	A1	19930618	FR 9215249	A	19921217	199337
US 5473201	A	19951205	US 92987351	A	19921207	199603
IT 1256714	B	19951215	IT 92MI2839	A	19921211	199627
DE 4141586	C2	19960711	DE 4141586	A	19911217	199632

Priority Applications (No Type Date): DE 4141586 A 19911217

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4141586	A1		5	B60R-016/02	
US 5473201	A		6	H02H-007/18	
DE 4141586	C2		5	B60R-016/02	
FR 2685142	A1			H02J-009/06	
IT 1256714	B			B60R-000/00	

Abstract (Basic): DE 4141586 A

The arrangement for a vehicle engine using an electronic control unit maintains a voltage supply for a short time after the engine is turned off via an ignition switch. The control unit is supplied from a battery via a key operated ignition switch and a resistor-capacitor T-network. The resistors form a series circuit, the capacitor connects their midpoints to earth.

A voltage limiting diode is connected between earth and the T-network input terminal. When the ignition key is turned off, the capacitor **discharges** through the second resistor, giving the control unit a further voltage decaying to zero for a period depending on the network time constant.

ADVANTAGE - Simple circuit, needing no additional relay.

Dwg.1/3

Abstract (Equivalent): US 5473201 A

1. In a control circuit means for controlling the after-running of an operating device in a motor vehicle, said motor vehicle being provided with an ignition circuit and a battery, said control circuit means comprising a voltage regulator having a control input connected with a terminal of the ignition circuit, said voltage regulator providing a supply voltage of the operating device, the improvement comprising means for changing a potential at the control input of the voltage regulator to end the after-running of the operating device occurring after **opening** the ignition circuit, the means for changing the potential at the control input of the voltage regulator includes a source of potential of the motor vehicle and at least one resistor **connecting electrically** the source of potential and the control input so that a duration of the after-running depends on a control signal of the operating device, the source of potential is the motor vehicle power supply and the resistor connecting the power supply and the control input is selected so that the voltage regulator is kept in the turned on state, and means for switching off the after-running of the operating device includes a transistor (T1) having an emitter, collector and a **base** and wherein the **base** of the transistor (T1) is **connected electrically** to receive the control signal of the operating device to terminate the after-running by shifting the transistor (T1) into a blocking state.

(Dwg.2/3

'33/3,AB/12 (Item 12 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c). 2004 Thomson Derwent. All rts. reserv.

009467372

WPI Acc No: 1993-160911/199320

XRPX Acc No: N93-123489

Capacitor **based** accelerometer for harsh environments - has ceramic **substrates** with capacitor formed on it and electrical circuit element assembled in layered form within rugged housing

Patent Assignee: TEXAS INSTR INC (TEXI )

Inventor: CHRISTENSEN D B; JOHNSON L K; KAWATE K W; MANDEVILLE R E;  
REIDEMEISTER E P; SOUTHWORTH R O

Number of Countries: 007 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 542436	A1	19930519	EP 92309630	A	19921021	199320 B
US 5345823	A	19940913	US 91790956	A	19911112	199436
EP 542436	B1	19960424	EP 92309630	A	19921021	199621
DE 69210179	E	19960530	DE 610179	A	19921021	199627
			EP 92309630	A	19921021	
JP 3210439	B2	20010917	JP 92263522	A	19921001	200156

Priority Applications (No Type Date): US 91790956 A 19911112

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
-----------	------	-----	----	----------	--------------

EP 542436	A1	E	17	G01P-015/125	
-----------	----	---	----	--------------	--

Designated States (Regional): DE FR GB IT NL

US 5345823	A		16	G01P-015/125	
------------	---	--	----	--------------	--

EP 542436	B1	E	20	G01P-015/125	
-----------	----	---	----	--------------	--

Designated States (Regional): DE FR GB IT NL

DE 69210179	E			G01P-015/125	Based on patent EP 542436
-------------	---	--	--	--------------	---------------------------

JP 3210439	B2		12	G01P-015/125	Previous Publ. patent JP 5223845
------------	----	--	----	--------------	----------------------------------

Abstract (Basic): EP 542436 A

The accelerometer includes a capacitor **based** detector (36) and an electronic circuit (18) housed in an insulated **base** (12).

The accelerometer has a capacitor detect plates (36.5) and a source plate defined inside and outside a groove on a **surface** of a ceramic **substrate**. The source plate (38.2) is attached to a flat metal member (38) and integral resilient beams.

The electrically insulating housing includes pins (14) extending through **openings** (36.9) in the accelerometer **substrate** and an electrical circuit to position the elements. The circuit is connected to the accelerometer with electrically conductive adhesive through guide **holes** (22.5).

ADVANTAGE - Provides reliable and responsive accelerometer in rugged and compact format.

Dwg.20/23

Abstract (Equivalent): EP 542436 B

An accelerometer comprising an electrically insulating ceramic **substrate** (36) having electrically conductive means on one **surface** (36.2) defining a capacitor detect plate (36.5), capacitor source plate connector means (36.6), and circuit path means (36.7) connected to the detect plate and to the source plate **connector** means; an **electrically** conductive metal plate member (38) having an attachment portion (38.1) secured in electrically conductive relation to the source plate connector means (36.6), a

capacitor source plate portion (38.2), and integral resilient beam means (38.3, 38.4) extending between the attachment and source plate portions supporting the source plate portion of the member in spaced relation to the detect plate to form a capacitor and to be movable relative to the detect plate in response to an acceleration force to provide an electrical signal; and signal conditioning electrical circuit means (18); characterised in that the accelerometer further includes a **base** (12) having integral pins (14) extending through **openings** (36.9, 18.4) in the **substrate** and the electrical circuit means securing the electrical circuit means in overlying relation to the plate member (38); and electrically conductive means (18.1) extending between the electrical circuit means and the **substrate electrically connecting** the **electrical** circuit means to the circuit path means on the **substrate** for conditioning the electrical signal to provide an output signal corresponding to the acceleration force.

(Dwg.20/23

Abstract (Equivalent): US 5345823 A

The accelerometer **unit** has a **capacitor** detect plate and a source place connector pref. defined respectively inside and outside a groove in one **surface** of a ceramic **substrate**. A flat metal member has an attachment portion secured in electrically conductive relation to the connector, a source plate portion being spaced over the detect plate to form a capacitor.

Integral resilient beams extend from the attachment portion to support the source plate portion spaced from the detect plate to be movable relative to the detect plate in response to an acceleration force to provide an electrical signal. Pref., glass rods between the attachment member portion and source place connector facilitate the spacing.

ADVANTAGE - Improved reliability and responsiveness as well as temperature independence. Compact, rugged structure adapted to withstand severe vehicle environment.

(Dwg.21/22

33/3,AB/13 (Item 13 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

008689413

WPI Acc No: 1991-193433/199126

XRPX Acc No: N91-148094

Power supply for copper vapour laser - has energy dissipation circuit with transformer to feed back excess electromagnetic energy via resistor to electronic switch input

Patent Assignee: COMMISSARIAT ENERGIE ATOMIQUE (COMS )

Inventor: GIDON S; HENNEVIN B; HENNEVIN B

Number of Countries: 015 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9108605	A	19910613				199126 B
FR 2654876	A	19910524				199133
EP 502067	A1	19920909	EP 90917674	A	19901122	199237
			WO 90FR839	A	19901122	
JP 5504443	W	19930708	WO 90FR839	A	19901122	199332
			JP 91500177	A	19901122	
EP 502067	B1	19940921	EP 90917674	A	19901122	199436
			WO 90FR839	A	19901122	
DE 69012834	E	19941027	DE 612834	A	19901122	199442

			EP 90917674	A	19901122	
			WO 90FR839	A	19901122	
US 5359279	A	19941025	WO 90FR839	A	19901122	199442
			US 92857929	A	19920518	

Priority Applications (No. Type Date): FR 8915423 A 19891123

Patent Details:

Patent No	Kind	Lang	Pg	Main IPC	Filing Notes
-----------	------	------	----	----------	--------------

WO 9108605	A				
------------	---	--	--	--	--

Designated States (National): JP US

Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LU NL SE

EP 502067	A1	F	36	H02J-007/02	Based on patent WO 9108605
-----------	----	---	----	-------------	----------------------------

Designated States (Regional): DE FR GB

JP 5504443	W			H01S-003/097	Based on patent WO 9108605
------------	---	--	--	--------------	----------------------------

EP 502067	B1	F	18	H02J-007/02	Based on patent WO 9108605
-----------	----	---	----	-------------	----------------------------

Designated States (Regional): DE FR GB

DE 69012834	E			H02J-007/02	Based on patent EP 502067
-------------	---	--	--	-------------	---------------------------

Based on patent WO 9108605

US 5359279	A		12	H01S-003/097	Based on patent WO 9108605
------------	---	--	----	--------------	----------------------------

Abstract (Basic): WO 9108605 A

The power supply unit(s) for a metallic vapour laser pulse supply uses a three phase bridge rectifier (D1, D2, D3, D4, D5, D6) to charge a **capacitor** (C1). This supply **unit** is connected to an electronic switch (K), a control circuit (cm) and a feedback transformer (T). A capacitor (C) is connected to the primary winding of the transformer (T) and across the input of the control circuit.

When the switch closes the capacitor is charged, the voltage across its terminals is compared to a step value by the control circuit and when the voltage across the capacitor reaches the step value the switch is opened. Any excess electromagnetic energy is dissipated in an energy absorbing circuit (26) via the secondary winding of the transformer (T).

ADVANTAGE - Has improved excess electrical energy dissipation circuit which improves stability characteristics of copper vapour lasers. (36pp Dwg.No.2/6

Abstract (Equivalent): EP 502067 B

The power supply unit(s) for a metallic vapour laser pulse supply uses a three phase bridge rectifier (D1, D2, D3, D4, D5, D6) to charge a **capacitor** (C1). This supply **unit** is connected to an electronic switch (K), a control circuit (cm) and a feedback transformer (T). A capacitor (C) is connected to the primary winding of the transformer (T) and across the input of the control circuit.

When the switch closes the capacitor is charged, the voltage across its terminals is compared to a step value by the control circuit and when the voltage across the capacitor reaches the step value the switch is opened. Any excess electromagnetic energy is dissipated in an energy absorbing circuit (26) via the secondary winding of the transformer (T).

ADVANTAGE - Has improved excess electrical energy dissipation circuit which improves stability characteristics of copper vapour lasers.

(Dwg.1)

EP-502067 Device for charging electrical energy storage means (C), this device being suitable for the pulsed electrical supply from a charge previously stored in the storage means and comprising: - DC electrical supply means (S) for these storage means; - switching means (K) which **connect** the DC **electrical** supply means (S) to the electrical energy storage means (C) and the closing of which makes the charging of the latter possible, - means (cm) for controlling the

switching means, - an inductive means (p) for temporarily storing magnetic energy, and - means provided for re-routing excess electrical energy, essentially of magnetic origin, likely to appear in the device in the course of charging the storage means (C), to means (S;26) capable of absorbing this excess electrical energy, thus avoiding sending this energy to the storage means, characterised in that the switching means are switching means having direct control for the **opening** and the closing, in that the control means are provided in order to compare the voltage at the terminals of the electrical energy storage means (C) with a defined voltage threshold and in order to cause the **opening** of the switching means when the threshold is reached by this voltage at the terminals of the storage means, and in that the device comprises a transformer (T) which includes: - a primary winding (p) forming the inductive means and connected, on one side, to the switching means (K), and on the other, to the electrical energy storage means (C) via a diode (d1) which prevents the latter from **discharging** to the DC electrical supply means (S), and - a secondary winding (s) which is provided for removing the excess electrical energy to the means (S;26) capable of absorbing the latter, and which is connected up, on one side, to these means via another diode (d2), the polarity of which makes this removal possible, and, on the other side, to a terminal of the DC electrical supply means.

(Dwg.1/6

Abstract (Equivalent): US 5359279 A

A pulse generator for supplying pulsed electrical energy from a charge stored in an accumulator is provided. The generator comprises a continuous electrical energy supply, an electrical energy accumulator, a switch for selectively connecting the supply means to the accumulator, and a switch control. The switch control compares voltages at the terminals of the accumulator with a given threshold voltage and controls the switch according to the comparison.

An inductor for temporary accumulation of magnetic flux energy and a diverter for diverting excess electrical energy to an energy absorber for absorbing the excess energy also are provided.

ADVANTAGE - Controls electrical energy stored in accumulation of generators.

Dwg.2/6

33/3,AB/14 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

007983630

WPI Acc.No: 1989-248742/198934

XRPX Acc No: N89-189425

Feedthrough type film capacitor - includes bellows-form dielectric film with inner and outer **surfaces** coated with electrodes, fixed axially compressed

Patent Assignee: MURATA MFG CO LTD (MURA )

Inventor: IMAGAWA S; OKUMURA M; SENDA A

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4845587	A	19890704	US 88271971	A	19881116	198934 B

Priority Applications (No Type Date): JP 87U175163 U 19871116

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 4845587	A	10		

Abstract (Basic): US 4845587 A

The through type film **capacitor** comprises a **capacitor unit** including a dielectric film in bellows form fixed in an axially compressed state. Electrode layers are formed on inner and outer **surfaces** of the dielectric film, the electrode layers being separated from each other at end faces of the dielectric film. A through terminal extends through the **capacitor unit** **electrically connected** to the inner electrode layer of the **capacitor unit**.

An earthing terminal plate has a planar shape and defines an **opening** for loosely receiving the through terminal. The earthing terminal plate is **electrically connected** to the outer electrode layer of the **capacitor unit**. The inner electrode layer of the **capacitor unit** is connected to the through terminal via a collector plate.

2a/7

33/3,AB/15 (Item 15 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

007660774

WPI Acc No: 1988-294706/198842

XRFX Acc No: N88-223678

**Panel** mounting connector with built-in filtering - has pins which pass through twin **disc** capacitor arrays, carry ferrite beads, and shielded by can

Patent Assignee: G & H TECHNOLOGY (GHTE-N); G&H TECHNOLOGY INC (GHTE-N)

Inventor: TANG T; TANG T P

Number of Countries: 017 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 287349	A	19881019	EP 88303316	A	19880413	198842 B
JP 1027171	A	19890130	JP 8889178	A	19880413	198910
US 4867706	A	19890919	US 8737505	A	19870413	198947
IL 86054	A	19910730				199133
CA 1292786	C	19911203				199204
EP 287349	B1	19920812	EP 88303316	A	19880413	199233
DE 3873591	G	19920917	DE 3873591	A	19880413	199239
			EP 88303316	A	19880413	

Priority Applications (No Type Date): US 8737505 A 19870413

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 287349	A	E	7		
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
US 4867706	A		4		
EP 287349	B1	E	8	H01R-013/719	
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE					
DE 3873591	G			H01R-013/719	Based on patent EP 287349

Abstract (Basic): EP 287349 A

A **panel** mounting connector body (88) houses a dielectric pin matrix (36) which is secured inside by a locking ring (90) and protected at its outer face by an insulating grommet (30). Within, it bears against a planar **disc** capacitor array (40). Beyond the capacitor array (40), selected pins carry one or more ferrite beads (50), and all are enclosed by an elastomer insert (58) which secures

the beads and provides inter-pin insulation. A seal (66) is placed against its exposed face.

A second capacitor array (72) follows the seal (66), and a grommet (78) placed beyond is covered by a second seal (82), all with **holes** for the pins. A sheet metal earthing can (10) surrounds the **capacitor units** (40,72) and provides connection with the body (88) via a spring-fingered ring (98).

ADVANTAGE - Comprehensive design of connector provides mechanical robustness, freedom from short-circuits, and adequate EMI filtering for designated pins.

4/4

Abstract (Equivalent): EP 287349 B

A multi-pin filtering **electrical connector** providing EMI filtering, for as many pins in the connector as desired, the filtering connector comprising: a multiplicity of electrical pins (24); a first non-conductive grommet seal (30) provided with **openings** for the pins, the first grommet seal being positioned at the outer face of a dielectric body (36); the dielectric body (36) having **openings** corresponding to the pins (24); a first planar ceramic capacitor array (40) having **openings** corresponding to the pins (24) and being positioned against the dielectric body (36); ferrite indicator beads (50) mounted on and around each of the pins (24) which is desired to be filtered; a non-conductive elastomer body (58) provided with **openings** to accept each of the beads (50) and each of the non-filtered pins, and to insulate the ferrite beads (50) from each other and from the first capacitor array (40), the elastomer body (58) being positioned against the first capacitor array; a first non-conductive interface seal (66), provided with **openings** for the pins, positioned against the outer face (62) of the elastomer body; a second planar ceramic capacitor array (72) having **openings** corresponding to the pins positioned against the first interface seal (66); a second non-conductive grommet seal (78), provided with **openings** for the pins (24), positioned at the outer face of the second capacitor array; a second non-conductive interface seal (82) provided with **openings** for the pins (24), positioned at the outer face of the second grommet seal (78); a conductive grounding cylinder (10) encircling the second grommet seal (78) and the first capacitor array (40) and also a portion of the dielectric body (36), and in electrical contact with the first capacitor array (40); a conductive shell (88) adapted for housing the pins (24), seals, dielectric body (36), elastomer body (58), capacitor arrays (40, 72) and grounding cylinder (10); and supported within the shell (88), a conductive ring element (96) providing a multiplicity of resilient contact fingers (98) for making electrical contact with the grounding cylinder (10) and providing an electrical grounding path from the pin array to the shell (88).

(Dwg. 4/4

Abstract (Equivalent): US 4867706 A

The filtering connector includes a multiplicity of electrical pins, each having a pin contact end (22) and an opposite end (24). It is to be understood that it is not necessary that all of the pins (20) be filtered. A mix of filtered pins and non-filtered pins may fit predetermined certain needs, although on occasion all pins may be filtered.

Positioned near the contact end of pin is a first non-conductive grommet seal (30) provided with **openings** for pins to pass through. The grommet (30) may be made from an electrically non-conductive elastomeric material, such as fluorosilicone rubber, for example. As used herein, 'non-conductive' and 'dielectric' are synonyms. A dielectric body (36) having **openings** corresponding to pins is

located after the grommet. The dielectric body (36), also referred to as a first insert, is preferably made from an epoxy moulding compound, sold under the trade designations Epiall or Fiberite, to enclose a portion of said pins (20) and to cushion against physical shocks.

(4pp

33/3,AB/16 (Item 16 from file: 350)  
DIALOG(R)File 350:Derwent.WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

004204931

WPI Acc No: 1985-031811/198505

XRPX Acc No: N85-023563

Decoupling capacitor mfr. using two-step moulding process - has hermetically sealed capacitive **unit** containing ceramic **capacitor**, leads and dummy pins for PCB insertion

Patent Assignee: ROGERS CORP (ROGR )

Inventor: SCHILLING D P

Number of Countries: 006 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 4494170	A	19850115	US 83551469	A	19831114	198505 B
DE 3441639	A	19850523	DE 3441639	A	19841114	198522
GB 2149970	A	19850619	GB 8428763	A	19841114	198525
FR 2554963	A	19850517				198529
BR 8405807	A	19850917				198543
GB 2149970	B	19871125				198747
IT 1177195	B	19870826				199033

Priority Applications (No Type Date): US 83551469 A 19831114

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 4494170	A		7		

Abstract (Basic): US 4494170 A

A number of active terminal pins are mechanically and **electrically electrically connected** to opposed conductive face **surfaces** of a capacitive element, the element being a dielectric body with opposed conductive face **surfaces**. The assembly is encapsulated in a moulding material with the active terminal pins projecting from the material the moulding step also including the formation of a number of cavities entirely in the moulding materials. Dummy pins are inserted in the cavities to form an intermediate premould element.

A second step is performed to mould a layer of material around the intermediate premould element to mechanically lock the dummy pins in the cavities, the pins being electrically isolated from the capacitive element. The active terminal pins are positioned in corresp. **openings** in moulds in each of the two moulding steps.

USE/ADVANTAGE - Especially for coupling between dual-in-line integrated circuit and pcb. Has small size.

3/4

Abstract (Equivalent): GB 2149970 B

A method of making a decoupling capacitor including the steps of: forming a subassembly of a generally flat capacitive element and a plurality of active terminal pins mechanically connected thereto, said capacitive element being a dielectric body with opposed major face **surfaces** which are conductive and to which the terminal pins are exclusively **electrically connected**; performnig a first

moulding step wherein said sub-assembly is encapsulated in an electrically insulating moulding material with said active terminal pins projecting therefrom, said first moulding step also including the formation of a plurality of cavities entirely in the moulding material; inserting dummy pins in said cavities to form an intermediate premould element; performing a second moulding step to mould a layer of electrically insulating moulding material around said intermediate premould element to mechanically lock said dummy pins in said cavities, said dummy pins being electrically isolated from said capacitive element.

33/3,AB/17 (Item 17 from file: 350)  
 DIALOG(R)File 350:Derwent WPIX  
 (c) 2004 Thomson Derwent. All rts. reserv.

004067850

WPI Acc No: 1984-213391/198434

XRAM Acc No: C84-089640

XRPX Acc No: N84-159756

Aluminium electrolysis process - uses crust breaking tool controlled by impedance measuring circuit

Patent Assignee: HEINZMANN U (HEIN-I); SCHWEIZ ALUMINIUM AG (SWAL )

Number of Countries: 014 Number of Patents: 010

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8403108	A	19840816	WO 84CH19	A	19840209	198434 B
DE 3305236	A	19840920	DE 3305236	A	19830216	198439
AU 8424373	A	19840830				198446
NO 8404033	A	19841227				198507
EP 135516	A	19850403	EP 84900604	A	19840209	198514
DE 3305236	C	19851121				198548
US 4563255	A	19860107	US 84667488	A	19841001	198605
EP 135516	B	19861015				198642
DE 3460987	G	19861127				198649
IT 1175323	B	19870701				199029

Priority Applications (No Type Date): CH 83739 A 19830210

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8403108	A	G			

Designated States (National): AU NO US

Designated States (Regional): AT BE CH DE FR GB LU NL SE

EP 135516	A	G
-----------	---	---

Designated States (Regional): AT BE CH DE FR GB LI LU NL SE

EP 135516	B	G
-----------	---	---

Designated States (Regional): AT CH DE FR GB LI NL SE

Abstract (Basic): EP 135516 A

Method for controlling a knock-in device with up/downwardly moving chisel (30) for the crust forming on the molten electrolyte (14) of a fusion electrolysis cell, by detection of the contacting of chisel/molten electrolyte, where signal variations effected by variations of the impedance between chisel and molten electrolyte are detected for control with the chisel (30) as measuring sensor in an electric measuring circuit, characterised in that the impedance between chisel (30) and molten electrolyte (14) is detected by means of an active impedance-measuring circuit (38,40,32,34).

(10pp)

DE 3305236 A

During the production of Al by electrolysis a **surface** crust is

for formed on top of the molten electrolyte bath. To maintain an **opening** in the crust for feeding alumina into the bath an air powered tool operates a punching chisel to break the crust. The tool is regulated by a control loop comprising an active signal source and an impedance measuring circuit. The impedance measurements and control circuitry provides precise regulation of the chisel.

In the idle position the chisel is raised clear of the bath and crust. In operation downward pressure is exerted on the chisel to contact the crust. Resistance to breakthrough is signalled through the control circuit to provide additional power to the chisel. After the chisel has broken through the crust and is in contact with the molten electrolyte the transmitted signal actuates the control system to return the chisel to the upper ideal position. The control circuitry is protected from the effects of the anode and cathode voltages and stray currents by means of capacitors in the circuit.

USE/ADVANTAGE - The power to operate the chisel is fully controlled thus avoiding any waste of excess energy. The chisel is raised clear of the bath when in the idle position thus avoiding the effects of corrosion and temperature. The control system will indicate any defects in the air supply or in the electrical insulation of the tool and anodes.

(14pp)

Abstract (Equivalent): EP 135516 B

Method for controlling a knock-in device with up/downwardly moving chisel (30) for the crust forming on the molten electrolyte (14) of a fusion electrolysis cell, by detection of the contacting of chisel/molten electrolyte, where signal variations effected by variations of the impedance between chisel and molten electrolyte are detected for control with the chisel (30) as measuring sensor in an electric measuring circuit, characterised in that the impedance between chisel (30) and molten electrolyte (14) is detected by means of an active impedance-measuring circuit (38,40,32,34).

Abstract (Equivalent): WO 8403108 A

During the production of Al by electrolysis a **surface** crust is formed on top of the molten electrolyte bath. To maintain an **opening** in the crust for feeding alumina into the bath an air powered tool operates a punching chisel to break the crust. The tool is regulated by a control loop comprising an active signal source and an impedance measuring circuit. The impedance measurements and control circuitry provides precise regulation of the chisel.

In the idle position the chisel is raised clear of the bath and crust. In operation downward pressure is exerted on the chisel to contact the crust. Resistance to breakthrough is signalled through the control circuit to provide additional power to the chisel. After the chisel has broken through the crust and is in contact with the molten electrolyte the transmitted signal actuates the control system to return the chisel to the upper idle position. The control circuitry is protected from the effects of the anode and cathode voltages and stray currents by means of capacitors in the circuit.

USE/ADVANTAGE - The power to operate the chisel is fully controlled thus avoiding any waste of excess energy. The chisel is raised clear of the bath when in the idle position thus avoiding the effects of corrosion and temperature. The control system will indicate any defects in the air supply or in the electrical insulation of the tool and anodes.

0/2

US 4563255 A

Crust breaker (28) for a fused salt electrolytic cell, partic. for Al production is controlled by an **electrical** circuit which **connects** the top **surface** of the breaker to a point (38) on the steel pot at cathode potential and is fed by an alternating current

from a source (32) providing an AC voltage of e.g. 24V. An electronic relay (34) measures a resultant AC signal which is a function of circuit impedance and emits a corresp. signal to the process control unit (36). Two neutralising **capacitors** (40) effect separation of the DC potential between the electrolytic cell and the process control or relay (34).

ADVANTAGE - Penetration of the crust is ensured by control of energy supplied to the breaker, the reliability of which is increased.  
(7pp)

33/3,AB/18 (Item 1 from file: 347)  
DIALOG(R)File 347:JAPIO  
(c) 2004 JPO & JAPIO. All rts. reserv.

07225770

#### CAPACITOR MOUNTING STRUCTURE

PUB. NO.: 2002-094210 [JP 2002094210 A]  
PUBLISHED: March 29, 2002 (20020329)  
INVENTOR(s): KIJIMA KENJI  
NAKAJIMA KIHEI  
APPLICANT(s): TOSHIBA CORP  
APPL. NO.: 2000-282196 [JP 2000282196]  
FILED: September 18, 2000 (20000918)

#### ABSTRACT

PROBLEM TO BE SOLVED: To provide a **capacitor mounting** structure which can increase the capacitance of a ceramic **capacitor** by connecting **unit** capacitances in series and parallel in a compact form with low-resistances.

SOLUTION: The **capacitor mounting** structure is provided with a plurality of **unit capacitors** 1 each of which is constituted by providing terminals 3 and 4 on a ceramic capacitor element 2 and a **substrate** 10 having a three-layer structure of electrodes 12 and 13 and an insulating layer 11 sandwiched between the electrodes 12 and 13. In one electrode 12 of the **substrate** 10, a plurality of **openings** 15 is formed and bosses 15 **electrically connected** to the other electrode 13 are respectively provided in the **openings** 15. The **unit capacitors** 1 are arranged on the electrode 12 and, at the same time, **electrically connected** in parallel with each other by bringing one terminals 3 of the capacitors 1 into contact with the electrode 12 and the other terminals 4 into contact with the other electrode 13 through the bosses 16.

COPYRIGHT: (C)2002, JPO

33/3,AB/19 (Item 2 from file: 347)  
DIALOG(R)File 347:JAPIO  
(c) 2004 JPO & JAPIO. All rts. reserv.

05914279

#### PRESSURE SENSOR MODULE

PUB. NO.: 10-197379 [JP 10197379 A]  
PUBLISHED: July 31, 1998 (19980731)  
INVENTOR(s): ISHIKAWA HIDETO  
NAKAO SATOSHI

TAKAGI SHIGEKIMI  
HAYASHI KAZUTAKA

APPLICANT(s): HOKURIKU ELECTRIC IND CO LTD [327816] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 08-351462 [JP 96351462]  
FILED: December 27, 1996 (19961227)

#### ABSTRACT

PROBLEM TO BE SOLVED: To provide a pressure sensor module in which through capacitors provided for a plurality of terminal members can be grounded through a simple structure.

SOLUTION: The pressure sensor module comprises a through **capacitor unit** 15 where through **capacitors** 27a-27c to be fitted with one end of terminal members 8a-8c are supported by a conductive supporting member 29 and the earth electrodes of the through capacitors 27a-27c are **connected electrically** with the conductive supporting member 29. The conductive supporting member 29 for the through **capacitor unit** 15 is provided with a pair of resilient contact members 31, 31. An **opening** for allowing the contacts of contact members 31, 31 to come into contact with an annular support 9 is made in the circumferential wall at the **base** of a connector body 7a. The contact members 31, 31 are constructed such that the contacts thereof are pressed against the inner circumferential **surface** of the annular support 9 through a spring force under a state where the annular support 9 is fitted over the **base** of the connector body 7a.

33/3,AB/20 (Item 3 from file: 347)

DIALOG(R)File 347:JAPIO

(c) 2004 JPO & JAPIO. All rights reserved.

05861782

CAPACITOR OF SEMICONDUCTOR MEMORY ELEMENT AND ITS MANUFACTURE

PUB. NO.: 10-144882 [JP 10144882 A]  
PUBLISHED: May 29, 1998 (19980529)  
INVENTOR(s): YAJIMA TSUKASA  
APPLICANT(s): OKI ELECTRIC IND CO LTD [000029] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 08-302108 [JP 96302108]  
FILED: November 13, 1996 (19961113)

#### ABSTRACT

PROBLEM TO BE SOLVED: To enlarge a stored electrostatic charge in a **capacitor** per memory cell **unit** area by providing a first lower part electrode **electrically connected** to a semiconductor **substrate** and a second tubular lower part electrode with an **opening** upward juxtaposed on a first lower part electrode.

SOLUTION: A first lower part electrode film 14 consisting of polycrystalline silicon is formed on a plane connected to an insulating film 12 piled on a **substrate** 11 through a contact 13, and an oxide film 15 is formed with the first lower part electrode film 14 selectively remaining on the part to form a capacitor. A second lower part electrode film 16 consisting of polycrystalline silicon is piled up a sacrificing oxide film 17. Next, the oxide film 15 and the sacrificing oxide film 17 are removed so as to form two tubular electrodes 16A in the rectangular shape over the whole plane. Thereby, a stored electrostatic charge in a memory capacitor can be enlarged without changing an occupying area and height of a memory cell.

.33/3,AB/21 (Item 4 from file: 347)  
DIALOG(R)File 347:JAPIO  
(c) 2004 JPO & JAPIO. All rts. reserv.

04432800

TANK TYPE GAS-BLAST CIRCUIT BREAKER

PUB. NO.: 06-076700 [JP 6076700 A]  
PUBLISHED: March 18, 1994 (19940318)  
INVENTOR(s): YONEZAWA TAKESHI  
APPLICANT(s): MITSUBISHI ELECTRIC CORP. [000601] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 04-230780 [JP 92230780]  
FILED: August 31, 1992 (19920831)  
JOURNAL: Section: E, Section Number 1564, Volume 18, Number 324, Pg. 11, June 20, 1994 (19940620)

ABSTRACT

PURPOSE: To provide a tank type gas-blast circuit breaker in which a **capacitor unit** can easily be mounted and modified and which is excellent in earthquake-resisting performance and is not affected by pollution while in atmosphere.

CONSTITUTION: An **opening** 23 is provided through part of a metallic tank 1 and is closed by a metallic closing member 24 in which a **capacitor unit** 25 having one terminal **electrically connected** to the inner **surface** of the member 24 is disposed. A **capacitor-unit** connecting member, comprising a first **connection** member 26 for **electrically connecting** either of conductors to the other terminal of the **capacitor unit** 25, a tulip contact 27 and a second connection conductor 28, is disposed in the metallic tank 1 when the **opening** of the tank is closed by the closing member.

33/3,AB/22 (Item 5 from file: 347)  
DIALOG(R)File 347:JAPIO  
(c) 2004 JPO & JAPIO. All rts. reserv.

00515648

COMPOSITE LC FILTER AND ITS MANUFACTURE

PUB. NO.: 55-003248 [JP 55003248 A]  
PUBLISHED: January 11, 1980 (19800111)  
INVENTOR(s): SHIMADA MORIYOSHI  
ONISHI TAKASHI  
APPLICANT(s): TAIYO YUDEN CO LTD [359306] (A Japanese Company or Corporation), JP (Japan)  
APPL. NO.: 53-075688 [JP 7875688]  
FILED: June 22, 1978 (19780622)  
JOURNAL: Section: E, Section Number 1, Volume 04, Number 28, Pg. 145, March 08, 1980 (19800308)

ABSTRACT

PURPOSE: To facilitate an easy assembling as well as to realize a miniature structure with facilitated manufacture for the composite LC filter obtained by forming a number of  $\pi$ -type filters into one body by improving the dielectric ceramic **substrate** which constitutes the capacitor block.

CONSTITUTION: Plural **units** of **capacitor** electrode 8 are formed independently near the pierced **hole** on one main **surface** of 1st dielectric ceramic **substrate** 5 on which several pierced **holes** are provided, and then capacitor electrodes 10 are formed in opposition to electrodes 8. Thus, the 1st capacitor block 1 is obtained. Then 2nd dielectric ceramic **substrate** 12 is formed with the pierced **holes** provided at the opposing positions to the pierced **holes** of block 1. Plural **units** of independent **capacitor** electrodes 15 are formed on the main **surface** of **substrate** 12, and capacitor electrodes 17 are provided on the other **surface** of **substrate** 12. Thus, 2nd capacitor block 2 is formed. Furthermore, plural units of circular ferrite 3 are distributed between blocks 1 and 2 to be **connected electrically** to electrodes 8 and 15 to be also fixed mechanically.

37/3,AB/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

6558271 INSPEC Abstract Number: A2000-10-7755-008, B2000-05-2860F-026

Title: PMN based thin film capacitor for decoupling applications in high speed digital circuits

Author(s): Fukumaru, F.; Nagakari, S.; Konushi, S.; Nishikawa, H.; Kamigaki, K.; Nambu, S.

Author Affiliation: R&D Centre, Kyocera Corp., Kagoshima, Japan

Conference Title: Ferroelectric Thin Films VII. Symposium p.573-8

Editor(s): Jones, R.E.; Schwartz, R.W.; Summerfelt, S.R.; Yoo, I.K.

Publisher: Mater. Res. Soc, Warrendale, PA, USA

Publication Date: 1999 Country of Publication: USA xvi+771 pp.

ISBN: 1 55899 447 5 Material Identity Number: XX-1999-02388

Conference Title: Ferroelectric Thin Films VII. Symposium

Conference Date: 30 Nov.-3 Dec. 1998 Conference Location: Boston, MA, USA

Language: English

Abstract: A new type of  $\text{Pb}(\text{Mg}/\text{sub } 1/3/\text{Nb}/\text{sub } 2/3/\text{O}/\text{sub } 3/(\text{PMN})$  based thin film decoupling capacitor for high speed digital circuits is presented. The thin film capacitor fabricated on a ceramic  $\text{Al}/\text{sub } 2/\text{O}/\text{sub } 3/$  substrate with **Ball Grid Array (BGA)**

terminations showed low impedance and low inductance characteristics in the 100 MHz-1 GHz range. The sol-gel derived  $\text{Pb}(\text{Mg}/\text{sub } 1/3/\text{Nb}/\text{sub } 2/3/\text{O}/\text{sub } 3/-\text{PbTiO}/\text{sub } 3/(\text{PMN-PT})$  thin film showed a high dielectric constant ( $k=3000$ ) with broad temperature dependence. The capacitor consists of a PMN-PT thin film (0.8  $\mu\text{m}$  thickness), Au electrodes, and **solder balls** mounted on the upper electrode as terminals. Numerical simulations based on the Partial Element Equivalent Circuit (PEEC) model were **conducted** for the design of electrodes, which gives low inductance of the capacitor. It was shown that the thin film 1.2 mm\*1.2 mm **capacitor mounted** on a board exhibits high capacitance of 20 nF, low ESR of 100 m  $\Omega$ , and low inductance of 135 pH. These values are in good agreement with the results of numerical simulations.

Subfile: A B

Copyright 2000, IEE

37/3,AB/2 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

015738791

WPI Acc No: 2003-800992/200375

Related WPI Acc No: 2003-361724

XRAM Acc No: C03-221050

XRPX Acc No: N03-641886

Semiconductor package e.g. **ball grid array** package has

chip **capacitor mounted** on mounting pad which is adhered

to inner ends of extended leads using **conductive** adhesive

Patent Assignee: ANZAI N (ANZA-I); TERUI M (TERU-I)

Inventor: ANZAI N; TERUI M

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020195705	A1	20021226	US 2001827246	A	20010406	200375 B
			US 2002211365	A	20020805	

Priority Applications (No Type Date): US 2001827246 A 20010406; US  
2002211365 A 20020805

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes  
US 20020195705 A1 61 H05K-007/06 Div ex application US 2001827246

Abstract (Basic): US 20020195705 A1

Abstract (Basic):

NOVELTY - The inner leads are extended inwardly to connect with a ground terminal and a power supply terminal. A chip **capacitor** (1310) is **mounted** on a mounting pad (1311) which is adhered to inner ends of the inner leads using **conductive** adhesive (1312), such that a decoupling capacitor is obtained.

USE - E.g. **ball grid array (BGA)** package  
and pin grid array (PGA) package.

ADVANTAGE - Power supply/ground noise is sufficiently reduced in the semiconductor.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor package.

die pad (1301)  
semiconductor chip (1303)  
bonding wire (1304)  
chip capacitor (1310)  
**conductive** adhesive (1312)  
pp; 61 DwgNo 29A/41

37/3,AB/3 (Item 2 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015140104

WPI Acc No: 2003-200631/200319

XRPX Acc No: N03-159833

Electronic assembly e.g. for telephone, has discrete capacitors comprising interior planes such that **conductive** terminals connected to interior planes of two adjacent discrete capacitors are laterally interconnected

Patent Assignee: INTEL CORP (ITLC )

Inventor: LI Y; CHUNG C

Number of Countries: 100 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020191368	A1	20021219	US 2001881342	A	20010614	200319 B
WO 2002103789	A2	20021227	WO 2002US18740	A	20020613	200319
US 6636416	B2	20031021	US 2001881342	A	20010614	200370

Priority Applications (No Type Date): US 2001881342 A 20010614

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

US 20020191368 A1 17 H01G-002/12

WO 2002103789 A2 E H01L-023/50

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA  
CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN  
IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ  
OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA  
ZM ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR  
IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

US 6636416 B2 H01G-004/228

Abstract (Basic): US 20020191368 A1

Abstract (Basic):

NOVELTY - An electronic housing has two discrete capacitors (504) which have several interior planes (602,604). The **conductive** terminals (608) electrically connected to interior planes (604) of the capacitors, are laterally interconnected.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) Electronic housing;
- (2) Electronic system; and
- (3) Electronic assembly manufacturing method.

USE - Electronic assembly e.g. integrated circuit package such as organic LGA package, plastic/flip chip PGA package, **BGA**/tape **BGA**/plastic **BGA**/flip chip **BGA**/flip chip tape. **BGA** package used in telephone, modem, cell phone, pager, radio, computer, television and monitors.

ADVANTAGE - By providing lateral connection between the capacitors, lateral inductance between the capacitors is reduced and high frequency current is effectively redistributed, thereby reducing system noise and the number of bypassing capacitors. Hence manufacturing yield is increased and manufacturing cost is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of the portion of the integrated circuit package and the surface mounted capacitors.

Discrete capacitor (504)  
Interior planes (602,604)  
**Conductive** terminals (608)  
pp; 17 DwgNo 6/16

37/3,AB/4 (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c). 2004. Thomson.Derwent. All rts. reserv.

014833796

WPI Acc No: 2002-654502/200270

XRPX Acc No: N02-517051

Electronic apparatus has **BGA** package with power supply pins and decoupling circuit board with multilayer capacitor provided on either surface of PCB and connected through **conductive** path

Patent Assignee: CISCO TECHNOLOGY INC (CISC-N)

Inventor: KOZAK F M; POMERLEAU R G

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6414850	B1	20020702	US 2000481139	A	20000111	200270 B

Priority Applications (No Type Date): US 2000481139 A 20000111

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6414850	B1	9	H05K-001/14	

Abstract (Basic): US 6414850 B1

Abstract (Basic):

NOVELTY - The apparatus has a **BGA** package (112) with power supply pins, that is provided on one surface of a printed circuit board (114). A decoupling board (412) having several **conductive** and dielectric layers to form multilayer capacitor structure, is provided on the other surface of the printed circuit board. A **conductive**

pathway is formed so as to connect the power supply pin and multilayer capacitor.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) Power supply pin decoupling method; and
- (2) Power supply pin decoupling apparatus.

USE - Electronic apparatus.

ADVANTAGE - Since the **conductive** pathway is formed between the power supply pin and multilayer capacitor, the need for PCB traces to interconnect decoupling capacitor to a high pin-count high density integrated circuit is eliminated and capacitor performance and design are improved. Also, since **BGA** device package and decoupling circuit board are arranged on either sides of printed circuit board, the space is effectively utilized and positioning and **mounting** of decoupling **capacitor** are performed easily.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of PCB used in electronic apparatus.

BGA package (112)

Printed circuit board (114)

Decoupling circuit board (412)

pp; 9 DwgNo 5/7

37/3,AB/5 (Item 4 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

014572740

WPI Acc No: 2002-393444/200242

XRFX Acc No: N02-308495

A method of embedding capacitors for an integrated circuit package includes **mounting capacitors** with one terminal connected to a **conducting** material on a first layer, and one terminal to a pad on a deposited non-**conducting** material

Patent Assignee: INTEL CORP. (ITLC )

Inventor: FIGUEROA D; HALE A; KOHMURA T; VRTIS J; WALK M; FIGUEROA D G;

HALE A D; VRTIS J K

Number of Countries: 096 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 200203463	A2	20020110	WO 2001US19225	A	20010614	200242 B
AU 200166944	A	20020114	AU 200166944	A	20010614	200242
US 6407929	B1	20020618	US 2000606882	A	20000629	200244
EP 1360721	A2	20031112	EP 2001944544	A	20010614	200377
			WO 2001US19225	A	20010614	

Priority Applications (No Type Date): US 2000606882 A 20000629

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 200203463 A2 E 31 H01L-023/498

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA  
CH CN CO CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS  
JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PL  
PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG US UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR  
IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW

AU 200166944 A H01L-023/498 Based on patent WO 200203463

US 6407929 B1 H05K-001/18

EP 1360721 A2 E H01L-023/498 Based on patent WO 200203463

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT

LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): WO 200203463 A2

Abstract (Basic):

NOVELTY - An electronic package (302) has **solder ball** connections (320, 322) to a circuit board (318) and an integrated circuit (314). The package has a first layer (304) with a **conductive** material (306) deposited on its top surface. **Capacitors** (308) are **mounted** with one terminal making contact with the **conductive** material. A non-**conductive** layer (310) is deposited and connections (312) are made between the other capacitor terminals and **conductive** pads (316) on the top surface.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) an electronic package including embedded capacitors

(b) and a computer system on a printed circuit board comprising a bus, a memory, an integrated circuit package including embedded capacitors, and a microprocessor located on the top surface of the package.

USE - The method of embedding capacitors is used for an integrated circuit package.

ADVANTAGE - The method provides for higher levels of capacitance at reduced inductance levels, suppressing noise, dampening power overshoot and droop, and supplying charge to die hot spots.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of an integrated circuit package including embedded capacitors.

Electronic package (302)

First layer (304)

**Conductive** material (306)

Capacitor (308)

Non-**conductive** layer (310)

Connection (312)

Integrated circuit (314)

**Conductive** pad (316)

Circuit board (318)

**Solder ball** connections (320, 322)

pp; 31 DwgNo 3/20

37/3,AB/6 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

013972570

WPI Acc No: 2001-456783/200149

Related WPI Acc No: 2001-380242

XRAM Acc No: C01-138122

XRPX Acc No: N01-338510

Circuit board having at least two by-pass capacitors giving reduced noise generation for semiconductor device

Patent Assignee: SHINKO DENKI KOGYO KK (SHIA ); SAKAGUCHI H (SAKA-I);

SASAKI M (SASA-I); SHINKO ELECTRIC IND CO LTD (SHIA )

Inventor: SAKAGUCHI H; SASAKI M

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010006119	A1	20010705	US 2000747397	A	20001222	200149 B
JP 2001185649	A	20010706	JP 99368652	A	19991227	200154
US 6603202	B2	20030805	US 2000747397	A	20001222	200353

Priority Applications (No Type Date): JP 99368652 A 19991227

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010006119	A1		44	H05K-001/16	
JP 2001185649	A		13	H01L-023/12	
US 6603202	B2			H01L-023/12	

Abstract (Basic): US 20010006119 A1

Abstract (Basic):

NOVELTY - A circuit board having at least two by-pass capacitors where a metallic foil is used in the formation of the electrode layer and is laminated to a ferroelectric material on the **mounted capacitor**.

DETAILED DESCRIPTION - Each by-pass capacitor has a first electrode layer formed in the uppermost layer of the circuit board, a ferroelectric layer formed from a ferroelectric material having a higher dielectric constant than the upper electrode layer, over the first electrode layer, and a second electrode layer formed over the ferroelectric layer.

The by-pass capacitor is manufactured by:

- (a) laminating metallic foil to ferroelectric material;
- (b) plating surface of ferroelectric material layer with metal to form first **conductor** layer;
- (c) selectively etching the first **conductor** layer to form the first electrode layer;
- (d) selectively etching the metallic foil to form second electrode layer opposing the first electrode layer;
- (e) removing the exposed area of the ferroelectric material to form by-pass capacitors having sandwich structure of first electrode layer, ferroelectric and second electrode layer, on resulting circuit board.

USE - A circuit board for use in production of semiconductor devices.

ADVANTAGE - Reduced noise generation and size allowing greater integration.

DESCRIPTION OF DRAWING(S) - Cross-sectional view of semiconductor.

ferroelectric layer (11)  
first electrode layer (16)  
pad (17)  
insulating layer (18)  
wiring pattern (21)  
second electrode layer (22)  
circuit board (24)  
by-pass capacitors (25)  
**solder ball** (26)  
semiconductor chip (27)  
solder (28)  
semiconductor device (30)  
pp; 44 DwgNo 2/14

37/3,AB/7 (Item 6 from file: 350)

DIALOG(R) File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

013056182

WPI Acc No: 2000-228050/200020

XRPX Acc No: N00-171268

Wiring **conductivity** inspection apparatus for resistor mounted on printed wiring board, judges **conduction** condition of wiring and

specifies defective location of wiring based on judgment result

Patent Assignee: SONY CORP (SONY )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 2000046914	A	20000218	JP 98214316	A	1998072	200020 B

Priority Applications (No Type Date): JP 98214316 A 19980729

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
JP 2000046914	A	17	G01R-031/28	

Abstract (Basic): JP 2000046914 A

NOVELTY - Inspection signal generation unit (5) generates an inspection signal (13) to a **conduction** inspection unit (24). The inspection result is fed back to a controller (3) through output terminal (9). **Conduction** condition of the wiring (14) is judged based on the inspection result. The controller specifies the defective location of the wiring based on the judgment result.

USE - For inspecting **conductivity** of wiring connected to IC such as **BGA**, CSP, resistor, **capacitor**, **mounted** on printed wiring board in computer.

ADVANTAGE - **Conduction** condition of the wiring is examined correctly and automatically. Defective location in the wiring are specified quickly. DESCRIPTION OF DRAWING(S) - The figure illustrates the block diagram of the wiring **conductivity** inspection apparatus. (3) Controller; (5) Inspection signal generation unit; (9) Output terminal; (13) Inspection signal; (14) Wiring; (24) **Conduction** inspection unit.

Dwg.1/23

42/3,AB/1 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015615968

WPI Acc No: 2003-678125/200364

Related WPI Acc No: 2003-779345

XRAM Acc No: C03-185169

XRFX Acc No: N03-541368

Test apparatus for integrated circuit wafer, comprises motherboard substrate, probe chip substrate, intermediate connectors, and probe chip carrier

Patent Assignee: CHONG F C (CHON-I); HAEMER J M (HAEM-I); LAHIRI S K (LAHI-I); MOK S (MOKS-I); SWIATOWIEC F J (SWIA-I); NANONEXUS INC (NANO-N)  
Inventor: CHONG F C; HAEMER J M; LAHIRI S K; MOK S; SWIATOWIEC F J; CHONG F ; SWIATOWIEC F

Number of Countries: 102 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030099097	A1	20030529	US 2001980040	A	20011127	200364 B
			US 2002178103	A	20020624	
WO 200401807	A2	20031231	WO 2003US19963	A	20030623	200402

Priority Applications (No Type Date): US 2002178103 A 20020624; US 2001980040 A 20011127

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030099097	A1	94	H05K-007/10	CIP of application US 2001980040	
WO 200401807	A2	E	H01L-000/00		

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20030099097 A1

Abstract (Basic):

NOVELTY - A test apparatus comprises:

- (i) motherboard substrate (I) having electrical **conductors** extending from bottom surface to top surface;
- (ii) a probe chip substrate having probe surface, connector surface, probe springs, electrical contacts, and electrical connections;
- (iii) intermediate connector(s) between (I) and probe chip substrate; and
- (iv) a probe chip carrier comprising compliant member

DETAILED DESCRIPTION - A test apparatus comprises a motherboard substrate, a probe chip substrate, intermediate connector(s), and a probe chip carrier. The mother substrate has bottom and top surfaces, and electrical **conductors** extending from bottom surface to top surface. The probe chip substrate has a probe surface, a connector surface, probe springs on the probe surface, electrical contacts on the connector surface, and probe chip electrical connections. Each probe spring is electrically connected to at least one contact through at least one probe chip electrical connection. The intermediate connector is located between the motherboard substrate and probe chip substrate

and includes electrically conductive connection(s) between each electrical contact on the probe chip substrate and each electrical conductor on bottom surface of motherboard substrate. The probe chip carrier is attached relative to the motherboard substrate and comprises a compliant member. The probe chip substrate is supported by the compliant member relative to the motherboard.

INDEPENDENT CLAIMS are also included for:

(a) A decal assembly process including providing a probe chip substrate and a compliant substrate having defined attachment region, and attaching the defined attachment region to the outer periphery of probe chip substrate;

(b) A package for connection to an integrated circuit device, comprising a package substrate, electrical connections extending through the package substrate between first and second substrate surfaces, and probe springs extending from the electrical connections and temporarily engageable to at least one integrated circuit device;

(c) A method of developing a probe assembly for connection to at least one device on a wafer, by providing a motherboard substrate and intermediate connector(s), providing a probe chip substrate design, receiving interconnection specification for the device on the wafer, and forming a probe chip substrate based on the substrate design;

(d) A probe assembly structure comprising a master slice having substrate(s) with standardized electrical connections, and at least one customized interface engageable to the master slice and comprising probe springs;

(e) An interposer comprising an interposer substrate, at least one electrically conductive via, electrically conductive first and second compliant probe springs, and at least one redundant electrically conductive element; and

(f) A process of forming an interposer by forming a first release layer on a substrate, forming electrically conductive stress layers on the first release layer having an inherent stress gradient comprising downward peeling stress, selectively forming a second release layer on the first stress layers, forming second electrically conductive stress layers on the second release layer having an inherent stress gradient comprising upward peeling stress, patterning at least one finger region in the first and second stress layers, selectively forming a compliant member having inner and peripheral region, attaching a rigid support ring to the peripheral region of compliant membrane to hold the membrane in tension, and etching the release layers.

USE - The apparatus is used for testing or burn-in of integrated circuit wafer.

ADVANTAGE - The apparatus provides tight signal pad pitch compliance and/or enables high levels of parallel testing in commercial wafer probing equipment. It enables high-speed testing in wafer form.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a bridge and leaf spring suspended probe card assembly.

Probe card (68)

Leaf spring (99)

Spacer (104,106)

Crash pad (120)

Pre-load assembly (121)

pp; 94 DwgNo 15/83

42/3,AB/2 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

015139718

WPI Acc.No: 2003-200245/200319

XRFX Acc No: N03-159447

**Capacitor** sheet for semiconductor device, has interface-connection feedthrough **conductors** in laminate through-holes and **capacitor**-connection feedthrough **conductors** in power source or ground electrode formation region

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU ); MATSUSHITA ELECTRIC IND CO LTD (MATU )

Inventor: ANDOH D; ECHIGO F; NAKAMURA T

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020182804	A1	20021205	US 2002155700	A	20020524	200319 B
JP 2003051427	A	20030221	JP 2002139150	A	20020514	200323

Priority Applications (No Type Date): JP 2001161928 A 20010530

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020182804	A1	13	H01L-021/8242		
JP 2003051427	A	8	H01G-004/38		

Abstract (Basic): US 20020182804 A1

Abstract (Basic):

NOVELTY - Interface-connection feedthrough **conductors** (4), are formed in through-holes passing through dielectric layer (1), power source electrode (2a) and ground electrode (2b) of a laminate sheet and are insulated by insulation walls (3). **Capacitor** -connection feedthrough **conductors** are formed only in either of the electrode formation regions and are connected with the corresponding electrodes.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:

- (1) **Capacitor** sheet production method;
- (2) Lamination board with **capacitor** sheet; and
- (3) Semiconductor device.

USE - **Capacitor** sheet for semiconductor device (claimed) of integrated circuit (IC) package including **ball grid array** (BGA) package and chip size package (CSP) used in electronic apparatus...

ADVANTAGE - Since the interface-connection feedthrough **conductors** and the **capacitor**-connection feedthrough **conductors** are independent, the length of the through-hole connection with the **capacitor** is minimized to suppress the influence of inductances of through-holes and to allow stabilization of power supply. The provision of through-holes passing through **capacitor** layer enables wiring connection in internal layers with high degree of freedom.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the **capacitor** sheet structure.

- Dielectric layer (1)
  - Power source electrode (2a)
  - Ground electrode (2b)
  - Insulation wall (3)
  - Feedthrough **conductors** (4)
- pp; 13 DwgNo 1/13

42/3,AB/3.. (Item 3 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

014470534

WPI Acc No: 2002-291237/200233

Related WPI Acc No: 2002-146918

XRAM Acc No: C02-085380

XRPX Acc No: N02-227388

IC device testing apparatus has probe tip placed on contact locations of test substrate, which is supported by polymer sheet having **holes** aligned with probe tip

Patent Assignee: BEAMAN B S (BEAM-I); FOGEL K E (FOGE-I); LAURO P A (LAUR-I); NORCOTT M H (NORC-I); SHIH D (SHIH-I); WALKER G F (WALK-I)

Inventor: BEAMAN B S; FOGEL K E; LAURO P A; NORCOTT M H; SHIH D; WALKER G F

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020011001	A1	20020131	US 98198179	A	19981123	200233 B
			US 2001972622	A	20011010	

Priority Applications (No Type Date): US 98198179 A 19981123; US 2001972622 A 20011010

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20020011001	A1	12	H05K-001/03	Div ex application US 98198179

Abstract (Basic): US 20020011001 A1

Abstract (Basic):

NOVELTY - Probe tips (13) are arranged on contact locations on a test substrate (10) which includes electro **conductor** patterns, a decoupling **capacitor** and elongated electrical **conductors**. **Holes** in a polymer sheet (40) supporting the probe tip, are aligned with the probe tips. When the substrate is moved towards integrated circuit (IC) device, **solder balls** on the IC device are receiving in the **holes**.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) (i) High density integrated rigid test probe fabrication method which involves bonding elongated electrical **conductor** to a substrate by forming a ball bond on the substrate. The elongated electrical **conductor** is sheared from ball bond and the exposed **conductor** end is flattened. The elongated **conductor** extends within **holes** in a polymer sheet on which another polymer sheet with **holes** is formed. The substrate is moved towards workpiece so that the elongated electrical **conductors** are placed in contact with **conductors** on the IC device; (ii) High density integral rigid test probe which includes short studs extending from ball bonds attached to contact locations of a fan out substrate which is selected from the group consisting of multi layer ceramic substrate with thick film wiring, multi layer ceramic substrate with thin film wiring, metallized ceramic substrates with thin film wiring, epoxy glass laminate substrates with copper wiring and silicon substrates with thin film wiring. The ball bonds and short studs are surrounded by a polymer sheet having coefficient of thermal expansion that is matched to the fan out substrate and has a glass transition temperature greater than 200 degrees C. Another polymer sheet with enlarged **holes** is formed over the polymer sheet. Two metal layers are formed on enlarged contact surface at the end of the studs to inhibit oxidation and diffusion of the temperatures up to 200 degrees C and to prevent out-diffusion of the underlying material

USE - For electrically testing an IC device and other electronic components that use **solder balls** for interconnection.

ADVANTAGE - The enlarged **holes** in the polymer sheet acts as a cup to control and contain the creep of the **solder balls** at high temperatures. The cup-shaped geometry of the probe facilitates alignment of **solder balls** with probe contact.

DESCRIPTION OF DRAWING(S) - The drawing shows the probe fabrication process.

test substrate (10)  
probe tip (13)  
polymer sheet (40)  
pp; 12 DwgNo 7/12

42/3,AB/4 (Item 4 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

003652627

WPI Acc No: 1983-12618K/198306

XRAM Acc No: C83-012191

XRPX Acc No: N83-023543

Low inductance chip **capacitor** with solder contacts - can be mounted on VLSI carrier as decoupling **capacitor**

Patent Assignee: IBM CORP (IBM C )

Inventor: DOUGHERTY W E; FEINBERG I; HUMENIK J N; PLATT A

Number of Countries: 007 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 70380	A	19830126	EP 82104815	A	19820602	198306 B
JP 58015219	A	19830128				198310
US 4439813	A	19840327	US 81285650	A	19810721	198415
CA 1182583	A	19850212				198511
EP 70380	B	19861001				198640
DE 3273531	G	19861106				198646

Priority Applications (No Type Date): US 81285650 A 19810721

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
-----------	------	--------	----------	--------------

EP 70380	A	E	15	
----------	---	---	----	--

Designated States (Regional): DE FR GB IT

EP 70380	B	E		
----------	---	---	--	--

Designated States (Regional): DE FR GB IT

Abstract (Basic): EP 70380 A

A chip **capacitor** comprises (a) sequentially, a bottom conductive layer (2), a dielectric layer (3), a top conductive layer (4) and an insulator layer (5); (b) a first via **hole** exposing the top **conductor**; (c) a second via **hole** extending through insulator, top **conductor** and dielectric to expose the bottom **conductor**; (d) a portion of the insulator layer extending about the sidewalls of the top **conductor** in the second via **hole**; and (e) isolated solder mounds (7) deposited on the insulator layer and in the via **holes**, contacting the exposed **conductor** layers.

The **capacitor** is made by (i) depositing bottom **conductor**

(2), dielectric (3) and top **conductor** (4) on a carrier substrate

(1); (ii) etching portions of the top **conductor** and dielectric to

expose the bottom **conductor**; (iii) depositing insulating material

(5) over the surfaces; (iv) etching the insulator to expose selected

portions of top and bottom **conductors** while maintaining them

mutually isolated; (v) depositing a layer (6) of ball limiting

metallurgy on selected exposed surfaces; and pref. (vi) depositing

**solder balls** (7) on selected areas to define contacts.

The low inductance **capacitor** is dimensionally compatible with VLSI packaging techniques, so can be directly mounted on the circuit board as decoupling **capacitor**, not spaced from the circuit as conventional.

.1A/4

42/3,AB/5 (Item 1 from file: 347)

DIALOG(R)File 347:JAPIO

(c) 2004 JPO & JAPIO. All rts. reserv.

07057274

NONREVERSIBLE CIRCUIT ELEMENT AND COMMUNICATION EQUIPMENT

PUB. NO.: 2001-284910 [JP 2001284910 A]

PUBLISHED: October 12, 2001 (20011012)

INVENTOR(s): HASEGAWA TAKASHI

OHIRA KATSUYUKI

APPLICANT(s): MURATA MFG CO LTD

APPL. NO.: 2000-099426 [JP 200099426]

FILED: March 31, 2000 (20000331)

#### ABSTRACT

PROBLEM TO BE SOLVED: To provide a nonreversible circuit element, which can be made low in height and avoids short-circuiting caused by a **solder ball**, and communication equipment using the element.

SOLUTION: While using a magnetic assembly 5 provided with a ferrite 54 and central **conductors** 51, 52 and 53 connected thereto in respectively different directions, chip **capacitors** C1, C2 and C3 and a chip resistor R are connected between the ports of the respective central **conductors** and a metal case 8 but by forming a **hole** closely to the terminal of a chip component to connect ports P1, P2 and P3 on the metal case 8, the generation of the **solder ball** is prevented and even when the **solder ball** is generated, short-circuiting between the terminal electrode and the metal case is prevented.

COPYRIGHT: (C)2001,JPO

46/3,AB/1 (Item 1 from file: 350)  
DIALOG(R) File 350;Derwent.WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015702400

WPI Acc No: 2003-764593/200372

Related WPI Acc No: 2002-302568

XRAM Acc No: C03-209833

XRPX Acc No: N03-612347

Fabrication of semiconductor package, e.g. **ball grid array** package, by attaching **semiconductor die** having bond pads to polymer film attached to lead fingers of metal lead frame, and wire bonding bond pads to lead fingers

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: MODEN W

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6589810	B1	20030708	US 99288423	A	19990408	200372 B
			US 2000546706	A	20000410	

Priority Applications (No Type Date): US 99288423 A 19990408; US 2000546706 A 20000410

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6589810	B1	12	H01L-021/44		Div ex application US 99288423 Div ex patent US 6310390

Abstract (Basic): US 6589810 B1

Abstract (Basic):

NOVELTY - Package fabrication includes providing a **semiconductor die** comprising bond pads, providing a metal lead frame comprising lead fingers, attaching a polymer film to lead fingers, attaching the **semiconductor die** to polymer film, wire bonding the bond pads to fingers, encapsulating the **semiconductor die** and lead fingers in encapsulating resin, and attaching ball contacts to the pads of lead fingers.

DETAILED DESCRIPTION - Fabrication of semiconductor package includes providing a **semiconductor die** comprising bond pads, providing a metal lead frame comprising lead fingers having pads in a grid **array** for attachment of **ball** contacts, attaching a polymer film to the lead fingers to support and electrically insulate the **semiconductor die** on the lead frame, attaching the **semiconductor die** to the polymer film, wire bonding the bond pads to the lead fingers, encapsulating the **semiconductor die** and lead fingers in an encapsulating resin having **openings** aligned with the pads, and attaching ball contacts to the pads.

USE - For fabricating semiconductor package, e.g. **ball grid array (BGA)** package.

ADVANTAGE - The inventive method provides improved semiconductor package.

DESCRIPTION OF DRAWING(S) - The figures are schematic cross-sectional views of **BGA** package fabrication.

**Semiconductor die** (12A)

**Conductors** (14C)

Ball bonding pads (28A)

Polymer **substrate** (50)

Beam leads (56)

Opening (58)  
Bumps (60)  
Bonding tool (66)  
pp: 12 DwgNo 5A, 5B, 5C/5

46/3,AB/2 (Item 2 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

015292090

WPI Acc No: 2003-353023/200333

XRAM Acc No: C03-093022

XRPX Acc No: N03-281969

Semiconductor package has **substrate** of approximate planar plate with insulative layer with land **holes** in its inner circumference and conductive patterns, **semiconductor die**, conductive bumps, encapsulating portion, and terminals

Patent Assignee: AMKOR TECHNOLOGY KOREA INC (AMKO-N); LEE K W (LEEK-I); LEE

S G (LEES-I); LEE S H (LEES-I); YANG Y (YANG-I)

Inventor: LEE S H; YANG J Y; LEE G U; LEE S G; LEE K W

Number of Countries: 002 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030006494	A1	20030109	US 2002186407	A	20020628	200333 B
KR 2003003539	A	20030110	KR 200139441	A	20010703	200333
KR 2003042819	A	20030602	KR 200173608	A	20011124	200366

Priority Applications (No Type Date): KR 200173608 A 20011124; KR 200139441 A 20010703

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030006494	A1		35	H01L-023/02	
KR 2003003539	A			H01L-023/52	
KR 2003042819	A			H01L-023/10	

Abstract (Basic): US 20030006494 A1

Abstract (Basic):

NOVELTY - Semiconductor package comprises a **substrate** of an approximate planar plate comprising:

- (i) an insulative layer having land **holes** in its inner circumference and conductive patterns on its **surface**;
- (ii) a **semiconductor die**;
- (iii) conductive bumps for coupling the bond pads to bond fingers of the conductive patterns;
- (iv) an encapsulating portion, and
- (v) terminals fused to each land

DETAILED DESCRIPTION - Semiconductor package comprises a **substrate** (110, 110', 110'') of an approximate planar plate comprising:

- (i) an insulative layer having land **holes** (108, 108', 108'') formed in its inner circumference, and electrically conductive patterns formed at a **surface** of the insulative layer and including bond fingers formed in a central portion of the insulative layer and several lands (104, 104', 104'') for covering the land **holes** connected to the bond fingers;
- (ii) a **semiconductor die** at a central portion of the **substrate** having bond pads formed at one **surface**;
- (iii) conductive bumps for coupling the bond pads to the bond fingers among the conductive patterns of the **substrate**;

(iv) an encapsulating portion formed by applying an encapsulant to the bond pads of the **semiconductor die**, the conductive bumps, and the bond fingers of the conductive patterns; and  
(v) terminals fused to each land of the **substrate**.

An INDEPENDENT CLAIM is also included for a method for manufacturing semiconductor package, which comprises providing an insulative layer of an approximately planar plate comprising a die cavity formed at its center and land **holes** formed at the periphery of the die cavity; coupling a conductive thin layer to the insulative layer; forming a **substrate** having electrically conductive patterns by etching the conductive thin layer in predetermined shape to form lands for covering the land **holes** and bond fingers extending to the inside of the die cavity; coupling an adhesive tape of an approximately planar plate to one **surface** of the **substrate**; locating a **semiconductor die** having bond pads inside the die cavity of the **substrate**; coupling conductive bumps to the bond pads; coupling the conductive bumps to the bond fingers; forming an encapsulating portion by applying an encapsulant to an inside of the die cavity to protect the bond pads of the **semiconductor die**, the conductive bumps, and the bond fingers of the **substrate** from external environment; removing the adhesive tape from the **substrate**; and coupling conductive balls to each land of the **substrate**.

USE - The semiconductor package may be used as a resin sealing package, a tape carrier package (TCP), a glass sealing package, or a metal sealing package. It can be an in-line type semiconductor package, e.g. dual in-line package or a pin grid array package; or a **surface** mount type semiconductor package, e.g. quad flat package, a plastic leaded chip carrier, a ceramic leaded carrier, or a **ball grid array** package.

ADVANTAGE - Partially inserting the **solder balls** into and connecting them to the land **holes** formed at the insulative layer of the **substrate** reduce the height of the **solder ball** to the minimum, thus reducing the thickness of the stack type **semiconductor** package. The **die** protective layer prevents the damage of the integrated circuits due to a transmission of a laser during the laser marking process of the semiconductor package, thus improving the quality of the marking process providing ease of handling.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a semiconductor package.

Semiconductor packages (100, 100', 100'', 200)

Lands (104, 104', 104'')

Land **holes** (108, 108', 108'')

**Substrate** (110, 110', 110'')

**Solder balls** (140, 140', 140'')

pp; 35 DwgNo 2/19

46/3,AB/3 (Item 3 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

014985263

WPI Acc No: 2003-045778/200304

Related WPI Acc No: 2003-695809

XRAM Acc No: C03-011582

XRPX Acc No: N03-035995

Board-on-chip package includes **conductors** and bonding sites on circuit side of **substrate**, and external contacts on back side of

**substrate** in electrical communication with **conductors**

Patent Assignee: CHAI L K (CHAI-I); HUI C C (HUIC-I); KUAN L C (KUAN-I);

MICRON TECHNOLOGY INC (MICR-N)

Inventor: CHAI L K; HUI C C; KUAN L C

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020100976	A1	20020801	US 2001774130	A	20010130	200304 B
US 6507114	B2	20030114	US 2001774130	A	20010130	200313

Priority Applications (No Type Date): US 2001774130 A 20010130

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20020100976	A1	13	H01L-021/44	
US 6507114	B2		H01L-023/48	

Abstract (Basic): US 20020100976 A1

Abstract (Basic):

NOVELTY - A board-on-chip (BOC) package (40) comprises a **substrate** (44) attached to a **semiconductor die** (42); **conductors** (64) on the circuit side (54) of the **substrate**; bonding sites (66) on the **conductors** extending from the edge; and external contacts on the back side (52) of the **substrate** in electrical communication with the **conductors**.

DETAILED DESCRIPTION - A BOC package comprises a **semiconductor die** comprising **die** contacts (50); a **substrate** attached to the die and having a circuit side and a back side; **conductors** on the circuit side; bonding sites on the **conductors** extending from the edge; external contacts on the back side in electrical communication with the **conductors**; an adhesive layer between the circuit side and the back side; wires (74) bonded to the die contacts and to the bonding sites; and an encapsulant (78) molded to the die and to the **substrate**, covering the wires. An INDEPENDENT CLAIM is included for a method for fabricating the above BOC package.

USE - As BOC package.

ADVANTAGE - The inventive BOC package has a reduced thickness and a smaller footprint than the prior art BOC package. It uses less encapsulant material, has less mold bleed, and a planar encapsulant **surface**.

DESCRIPTION OF DRAWING(S) - The figure is an enlarged cross-sectional view of the inventive BOC package.

BOC) package (40)

Die (42)

**Substrate** (44)

Die contacts (50)

Back side (52)

Circuit side (54)

Solder mask (60)

**Openings** (62)

**Conductors** (64)

Bonding sites (66)

Conductive vias (68)

Wires (74)

Encapsulant (78)

pp; 13 DwgNo 2B/4

46/3,AB/4 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

014649326

WPI Acc No: 2002-470030/200250

XRAM Acc No: C02-133613

XRPX Acc No: N02-370981

Semiconductor apparatus for providing **semiconductor die** to external fiber optic cable connection, comprises **semiconductor die**, integrated circuit, module, opto-electric device and electrical **conductor(s)**

Patent Assignee: NAT SEMICONDUCTOR CORP (NASC )

Inventor: DEANE P; MURRAY C; NGUYEN L; TSAY C

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6364542	B1	20020402	US 2000568094	A	20000509	200250 B

Priority Applications (No Type Date): US 2000568094 A 20000509

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6364542	B1	11	G02B-006/36	

Abstract (Basic): US 6364542 B1

Abstract (Basic):

NOVELTY - A semiconductor apparatus comprises a **semiconductor die** (30) having a **surface**, an integrated circuit fabricated on the die **surface**, a module (16) mounted onto a package encapsulating the die and adapted to receive an external fiber optic cable, an opto-electric device (46) housed in the module, and electrical **conductor(s)** coupled between the integrated circuit and opto-electric device.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method for manufacturing the above apparatus by encapsulating a **semiconductor die** with an integrated circuit fabricated into a package where a module with an opto-electric device is mounted, and providing a direct electrical connection between the opto-electric device and the integrated circuit on the die.

USE - For providing **semiconductor die** to external fiber optic cable connection.

ADVANTAGE - The low cost apparatus effectively provides the **semiconductor die** to the external fiber optic connection.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of the semiconductor apparatus.

Module (16)

Fiber optic cable (18)

**Semiconductor die** (30)

**Solder ball** (36)

Translucent material (43)

**Base** (44)

Opto-electric device (46)

Mirror (48)

Adhesive (50)

pp; 11 DwgNo 5/5

46/3,AB/5 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

014481865

WPI Acc No: 2002-302568/200234  
Related WPI Acc No: 2003-764593; 2003-851499  
XRAM Acc No: C02-088054  
XRPX Acc No: N02-236610

A semiconductor package, especially **BGA** package comprising a  
**semiconductor die**, several **conductors**, a polymer tape,  
an encapsulating resin and several ball contacts

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: MODEN W

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6310390	B1	20011030	US 99288423	A	19990408	200234 B

Priority Applications (No Type Date): US 99288423 A 19990408

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6310390	B1	12	H01L-023/495		

Abstract (Basic): US 6310390 B1

Abstract (Basic):

NOVELTY - A semiconductor package comprising a **semiconductor die**, several **conductors** attached to the die, a polymer tape attaching the die to the **conductors**, a resin encapsulating the package and several ball contacts in the **openings** on one side of the package.

DETAILED DESCRIPTION - The semiconductor package (I) comprises:

- (a) A **semiconductor die**;
- (b) Several **conductors** attached to the die comprising lead fingers of a metal lead frame, **conductors** on one side having a first width W1, **conductors** on the other having a second width W2, W1 being less than W2. The first side including several first pads wire bonded to the die, the second side including several second pads configured in a dense array of rows and columns;
- (c) A polymer tape attaching the die to the **conductors** for wire bonding and electrically insulating the **conductors**;
- (d) A resin encapsulating the die and the **conductors** and having several **openings** aligned with the second pad; and
- (e) A plurality of ball contacts in the **openings** attached to the second pads.

USE - Used as a semiconductor package, especially **BGA** package.

DESCRIPTION OF DRAWING(S) - Figure 1C is a cross sectional view of the **BGA** package. Figure 1D is a schematic plan view taken along line 1D-1D.

**BGA** package (10)  
**semiconductor die** (12)  
internal **conductors** (14)  
external ball contacts (16)  
encapsulating resin (18)  
bond pads (20)  
face side (22)  
back side (24)  
bonding pads (26)  
ball bonding pads (28)  
bond wires (30)  
lead fingers (32)  
lead frame (34)  
polymer tape (36)  
common axes (38L, 38R)

pp; 12 DwgNo 1C, 1D/24

46/3,AB/6 (Item 6 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

014342419

WPI Acc No: 2002-163122/200221  
Related WPI Acc No: 2001-396558  
XRAM Acc No: C02-050291  
XRPX Acc No: N02-124481

Semiconductor package fabrication method e.g. for **ball grid array** package, involves forming metal bumps through **openings** of polymer **substrate**, onto bonding **holes** of **conductor** and pads, to connect pad and **conductor**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)  
Inventor: CORISIS D; MODEN W  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6329222	B1	20011211	US 98206116	A	19981204	200221 B
			US 99467643	A	19991220	

Priority Applications (No Type Date): US 98206116 A 19981204; US 99467643 A 19991220

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6329222	B1	11	H01L-021/44		Div ex application US 98206116 Div ex patent US 6232666

Abstract (Basic): US 6329222 B1  
Abstract (Basic):

NOVELTY - A polymer **substrate** (32) comprising **openings** and several **conductors** (36) with bonding **holes** is bonded to the **semiconductor die**, so that the bonding **holes** align with pads arranged on the **semiconductor die**. Metal bumps are formed through the **openings**, onto the bonding **holes** and on the pad to electrically connect the pad and **conductors**.

USE - For fabricating semiconductor package such as **ball grid array** package.

ADVANTAGE - Enables improved **BGA** fabrication and provides an improved interconnect with polymer **substrates**.

DESCRIPTION OF DRAWING(S) - The figure shows a plan view of interconnect.

Polymer **substrate** (32)

**Conductors** (36)

pp; 11 DwgNo 2/5

46/3,AB/7 (Item 7 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

014056695

WPI Acc No: 2001-540908/200160  
Related WPI Acc No: 2000-363552  
XRAM Acc No: C01-161359  
XRPX Acc No: N01-402015

Fabrication of semiconductor package involves using **substrate** having mask defining open die attach area

Patent Assignee: JIANG T (JIAN-I); SCHROCK E (SCHR-I)

Inventor: JIANG T; SCHROCK E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010013642	A1	20010816	US 98191215	A	19981112	200160 B
			US 99258961	A	19990301	

Priority Applications (No Type Date): US 98191215 A 19981112; US 99258961 A 19990301

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010013642	A1	13	H01L-023/495	Div ex application US 98191215	Div ex patent US 6048755

Abstract (Basic): US 20010013642 A1

Abstract (Basic):

NOVELTY - A semiconductor package is fabricated by providing a **substrate** having first **surface** (44) with die attach area, depositing photoimageable mask material on **substrate** (56), exposing and developing the mask material to form mask with an **opening** on the die attach area, placing a **semiconductor die** in the **opening**, and bonding the die attach area.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(A) a semiconductor lead frame comprising a **substrate** having **surfaces**, **conductors** formed on a first **surface**, a first mask formed on the first **surface** having via **openings** to the **conductors**, and a second mask formed on second **surface** comprising **opening** defining a die attach area on the **substrate**; and

(B) a **substrate** for fabricating a semiconductor package.

USE - The method is used for fabricating semiconductor package.

ADVANTAGE - The open die attach area permits the die to bonded directly to the **substrate** than to the solder mask. This improves adhesion of the die to the **substrate**, reduces trapped moisture, and prevents delamination of the solder mask in the die attach area.

DESCRIPTION OF DRAWING(S) - The figure is a plan view of a panel containing **substrate**.

First **surface** (44)

**Substrate** (56)

pp; 13 DwgNo 2A/7

46/3,AB/8.. (Item 8 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

013673630

WPI Acc No: 2001-157842/200116

Related WPI Acc No: 1998-239236; 1999-080446; 1999-312281; 2000-430262; 2000-474854; 2001-209931; 2001-256995; 2001-475257; 2001-541000; 2001-646957; 2002-129435; 2002-255438; 2002-402153; 2002-705790; 2003-899806; 2004-080037

XRFX Acc No: N01-114859

Micromachined chip scale package for **semiconductor die**, has **discrete** preformed blank placed over passivation layer on active **surface** of **semiconductor die** and secured using bonding

material

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)  
Inventor: AKRAM S; FARNWORTH W M; HEMBREE D R  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6124634	A	20000926	US 96612059	A	19960307	200116 B
			US 98156300	A	19980917	

Priority Applications (No-Type Date): US 96612059 A 19960307; US 98156300 A 19980917

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6124634	A		9	H01L-023/58	Cont of application US 96612059

Abstract (Basic): US 6124634 A

Abstract (Basic):

NOVELTY - The chip scale package (10) has a **discrete** preformed blank placed over the passivation layer (18) on the active **surface** (14) of a **semiconductor die** (12), and secured using a bonding material (24) to form a layer of **semiconductor die**, passivation layer and **discrete** preformed blank.

DETAILED DESCRIPTION - The **semiconductor die** includes an integrated circuit with bond pads (16) on its active **surface** on which the passivation layer is disposed. The **discrete** preformed blank is made of semiconductor material similar to the composition of the **semiconductor die**. The bondable **surface** of the **discrete** preformed blank has **surface** dimensions not in excess of the **surface** dimensions of the active **surface** of the **semiconductor die**. **Apertures** (22) are preformed on the **discrete** preformed blank for accessing the bond pads of the **semiconductor die**.

USE - For **semiconductor die**.

ADVANTAGE - Can be executed at **wafer** level. Can be used to reroute bond pads for flip-chip direct die connect (DOC) and direct die attach (DDA) use. Advantageous for formation and use of **solder** or conductive epoxy **balls** or bumps in flip-chip format. Readily adaptable to stacking of dies to form multi-die circuits. Includes trenches that may function as alignment components for clips contacting new bond pads associated with trenches. Can replace multi-chip module (MCM) e.g. single in-line memory module (SIMM). Can be attached face-to-face against opposing sides of **conductor**-carrying **substrate** or face-to-face against each other. Employs suitable edge-connect structure for external connections to a circuit.

DESCRIPTION OF DRAWING(S) - The figure shows the side sectional elevation of the micomachined chip scale package.

Chip scale package (10)

**Semiconductor die** (12).

Active **surface** (14)

Bond pads (16)

Passivation layer (18)

**Apertures** (22)

Bonding material (24)

pp; 9 DwgNo 2/10

46/3,AB/9 (Item 9 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

013474526

WPI Acc No: 2000-646469/200062

Related WPI Acc No: 2002-048212; 2002-121366; 2002-236952; 2002-499304

XRAM Acc No: C00-195441

Electronic devices encapsulation for **substrate-based conductor** grid array packages involves injecting thermosetting resins into upper and lower mold cavity portions to separately encapsulate **semiconductor dies**

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: THUMMEL S G

Number of Countries: 001 ..Number of Patents: 001.. . . . .

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6117382	A	20000912	US 9819226	A	19980205	200062 B

Priority Applications (No Type Date): US 9819226 A 19980205

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6117382	A	18	B29C-070/70	

Abstract (Basic): US 6117382 A

Abstract (Basic):

NOVELTY - Upper and lower mold plates (12,14) are moved towards each other to form mold cavity so that mold plates engages respective **surfaces** (48A,48B) of **substrates** (18A,18B). Thermosetting resins (30,40) are injected into upper and lower mold cavity portions (16A,16B) to separately encapsulate **semiconductor dies** (52A,52B) on **surfaces** of **substrate**, respectively.

DETAILED DESCRIPTION - The **substrates** with encapsulated **semiconductor dies** are removed from respective mold plates. **Semiconductor dies** (52A,52B) are provided on **surfaces** (48A,48B) of **substrates** (18A,18B) respectively. Upper and lower mating mold plates have respective mold cavity portions. Each mold cavity portion has feed runners (24,34) leading from material supply to mold cavity portion. The **substrates** with **semiconductor dies** are placed in back to back orientation between upper and lower mold plates. Each mold cavity portion of mold plates is connected to vent runner for **opening** mold cavity portion. Thermosetting resin (40) is of same or different material from that of resin (30). The resins are injected simultaneously or at different times into upper and lower mold cavity portions. Backsides (56A,56B) of **substrates** containing solder bumps are cleaned and electronic devices are cured at an elevated curing temperature.

USE - Used for encapsulating electronic devices within mold cavity for wide variety of **substrate based conductor grid array** packages such as **ball grid array** (**BGA**), pin grid array (**PGA**), land grid array (**LGA**) including those mounted on monolayer **substrates**, multilayer circuit board **substrates** and multichip modules (**MCM**).

ADVANTAGE - Enables doubling production rate effectively and encapsulation of devices with different **substrate** thickness is performed without adjustment of mold plate spacing. Electronic devices can be encapsulated back to back simultaneously within a single mold cavity so number of packages encapsulated in mold machine is doubled without any significant increase in packaging cycle time.

DESCRIPTION OF DRAWING(S) - The figure shows cross-section of molding machine.

Upper and lower mold plates (12,14)

Upper and lower mold cavity portions (16A,16B)

**Substrates** (18A,18B)

Feed runners (24,34)  
Thermosetting resins (30,40)  
**Substrate surface** (48A,48B)  
**Semiconductor dies** (52A,52B)  
Backsides (56A,56B)  
pp; 18 DwgNo 1/12

46/3,AB/10 (Item 10 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

013438682

WPI Acc No: 2000-610625/200058  
Related WPI Acc No: 2002-338321; 2003-101814  
XRPX Acc No: N00-452138

Chip scale semiconductor package, has flux circuit whose **openings**  
align with contact die's reflow ball of **semiconductor die** for  
connecting contact die to external contact

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)  
Inventor: BROOKS M; FARNWORTH W M; WOOD A G  
Number of Countries: 001 Number of Patents: 001  
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6097087	A	20000801	US 97961881	A	19971031	200058 B

Priority Applications (No Type Date): US 97961881 A 19971031

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6097087	A		10	H01L-023/04	

Abstract (Basic): US 6097087 A

Abstract (Basic):

NOVELTY - **Semiconductor die** (32) has **die** contacts  
(48) with reflow balls on the face. Flux circuit (34B) attached to the  
face has polymer **substrate** with two sides having **openings**  
(64,66) aligned with reflow balls and having external contact (40) on  
one side and **conductor** (38A) on other side. The compressed  
**solder balls** (86C) connect **conductor** and die contact  
has reflow balls (86A) in the **opening** (64).

USE - In chip scale package e.g. **BGA**, **FPGA**.

ADVANTAGE - Improves interconnection between the external contacts  
and contact on the die by avoiding stress and the connectors. External  
contact with dense array is achieved by using **solder balls**.

DESCRIPTION OF DRAWING(S) - The figure shows the enlarged schematic  
cross-sectional view of chip scale semiconductor package.

**Semiconductor die** (32)

Flux circuit (34B)

**Conductor** (38A)

External contacts (40)

Die contacts (48)

**Openings** (64,66)

Reflow balls (86A)

Compressed **solder balls** (86C)

pp; 10 DwgNo 9D/13

46/3,AB/11 (Item 11 from file: 350)  
DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

013191679

WPI Acc No: 2000-363552/200031

Related WPI Acc No: 2001-540908

XRAM Acc No: C00-109757

XRFX Acc No: N00-271923

**Ball grid array** package fabrication, involves bonding **semiconductor die** directly to **substrate** through adhesive layer by inserting **semiconductor die** into **opening** in mask

Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)

Inventor: JIANG T; SCHROCK E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6048755	A	20000411	US 98191215	A	19981112	200031 B

Priority Applications (No Type Date): US 98191215 A 19981112

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6048755	A	12	H01F-021/00	

Abstract (Basic): US 6048755 A

Abstract (Basic):

NOVELTY - Several **conductors** (48) and die attach area (50) are formed on the **surfaces** (44,46) of a **substrate** (56). Photoimageable mask material is deposited on both the **surfaces** which is exposed and developed to form solder masks (80A,80B). The mask on the die attach area side is formed with an **opening** (86) with an outline the same as that of **semiconductor die** (16) for bonding it directly using an adhesive layer (72).

DETAILED DESCRIPTION - Several **conductors** are provided on the **surface** (44) of the **substrate** and die attach area is provided on the other **surface** (46) of a **substrate** (56). A photoimageable mask material is deposited on both the **surfaces** which is exposed and developed to form masks on both the **surfaces** respectively. The die attach area is formed with an **opening** for attaching a **semiconductor die** (16) directly to the **substrate** using an adhesive layer (72). The die and the mask are encapsulated by an encapsulating resin. The **substrate** is formed with wire bonding **openings** (64) for wiring (94) between the die and the **conductors**. Multiple through-holes (54) are formed in the **conductor** side mask for bonding **solder balls** (88) to the **conductors**. A glob top (92) is formed on wire bonding **opening** and on the wires.

USE - For fabrication of **ball grid array** (BGA) packages.

ADVANTAGE - The die bonding improves the adhesion of die to **substrate** thereby reducing trapped moisture and preventing delamination of solder mask in the die attach area.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic cross sectional view of completed **BGA** package.

**Semiconductor die** (16)

**Surfaces of substrate** (44,46)

**Conductor** (48)

**Die attach area** (50)

**Substrate** (56)

**Opening** (64)

**Adhesive layer** (72)

**Solder masks** (80A,80B)

Opening (86)  
Solder balls (88)  
Encapsulating resin (90)  
Glob top (92)  
Wiring (94)  
pp; 12 DwgNo 7/7

46/3,AB/12 (Item 12 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

012557235

WPI Acc No: 1999-363341/199931

XRPX Acc No: N99-271349

Fixing method of chip sized package semiconductor device e.g. land grid array, ball grid array semiconductor device - involves filling sealing resin into non-packing fraction of die bonding agent

Patent Assignee: MITSUI HIGH TEC KK (MIHI )

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 11135669	A	19990521	JP 9841414	A	19980207	199931 B

Priority Applications (No Type Date): JP 97247670 A 19970827

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 11135669	A		5	H01L-023/12	

Abstract (Basic): JP 11135669 A

NOVELTY - A semiconductor device (14) is joined to the upper surface of first insulation layer (11) through die bonding agent (13) which does not overflow on the side of semiconductor device. Non-packing fraction of the die bonding agent is filled with sealing resin (21). DETAILED DESCRIPTION - Opening is formed on the perimeter of first insulation layer. Conductor circuit pattern (12) provided with several leads (15) is provided on the backside of first insulation layer. A bonding wire (18) connects each pad (17) and exterior connecting terminal (16) of the semiconductor device. The exterior connecting terminal is connected to inner side connecting terminals (19) of each lead of the circuit pattern. The device, bonding wire and exterior connecting terminal are covered by sealing resin. A second insulation layer (22) covers the circuit pattern except the external connecting terminal.

USE - For fixing chip sized package (CSP) semiconductor device e.g. land grid array (LGA), ball grid array (BGA) semiconductor device.

ADVANTAGE - Promotes heat dissipation of semiconductor device. Forms narrow perimeter part of semiconductor device. DESCRIPTION OF DRAWING(S) - The figure is sectional view of chip sized package semiconductor device. (11) Insulation layer; (12) Conductor circuit pattern; (13) Die bonding agent; (14) Semiconductor device; (15) Lead; (16) Exterior connecting terminal; (17) Pad; (18) Bonding wire; (19) Inner side connecting terminal; (21) Sealing resin.

Dwg.1/3

46/3,AB/13 (Item 13 from file: 350)  
DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

012077995

WPI Acc No: 1998-494906/199842

XRPX Acc No: N98-386527

Circuit board for IC package e.g. **BGA** package - has utility region comprising ring-like power traces and ground traces formed alternatively, that are connected to respective **solder balls** via through **holes** with conductive material

Patent Assignee: ACC MICROELECTRONICS CORP (ACCM-N)

Inventor: CHU E; LAI H

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5801440	A	19980901	US 95541423	A	19951010	199842 B
TW 347582	A	19981211	TW 95111143	A	19951021	199920

Priority Applications (No Type Date): US 95541423 A 19951010

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5801440	A	9	H01L-023/52	
TW 347582	A		H01L-023/28	

Abstract (Basic): US 5801440 A

The circuit board has a **semiconductor die** attachment region (12) on one side of an insulated **substrate**. An utility region (22) surrounds the die attachment region. The utility region includes ring-like ground traces (18) and power traces (24) extended alternately. A single trace region (36) that surrounds the utility region, includes a set of signal traces (40) connected to the **semiconductor die** via **conductors**.

**Solder balls** for connecting to a power source and for earthing are provided on the reverse side of the **substrate**. A set of through **holes** with conductive material are formed in the **substrate**, that connect the ground traces and power traces to respective **solder balls**.

ADVANTAGE - Enables efficient usage of signal traces for conducting electrical signals. Reduces signal noise. Reduces required length of wire bond by enabling close arrangement of bonding regions as there is no one to one correspondence between input/output pads and bonding regions.

Dwg.1/5

46/3,AB/14 (Item 14 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

011173881

WPI Acc No: 1997-151806/199714

Related WPI Acc No: 1996-511344

XRAM Acc No: C97-048512

XRPX Acc No: N97-125560

**BGA** type semiconductor device mfg method - involves attaching **conductor circuit substrate** and semiconductor circuit element to metal **substrate** frame by thermocoupling process

Patent Assignee: MITSUI HIGH TEC KK (MIHI ); MITSUI HIGH TEC INC (MIHI )

Inventor: NAKASHIMA T; TAKAI K; TATEISHI K

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
-----------	------	------	-------------	------	------	------

JP 9027563	A	19970128	JP 95136019	A	19950509	199714	B
US 5661086	A	19970826	US 96584299	A	19960111	199740	

Priority Applications (No Type Date): JP 95136019 A 19950509; JP 9596064 A 19950328

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9027563	A		8	H01L-023/12	
US 5661086	A		16	H01L-021/48	

Abstract (Basic): JP 9027563 A

The method involves forming a metal **substrate** frame (11) with a semiconductor circuit element mounting area (11b). A **conductor** circuit **substrate** frame which consists of a **conductor** circuit **substrate** (13) with a **conductor** circuit pattern (13c) is formed, separately. Then, thermocompression bonding of the **conductor** circuit **substrate** onto the metal **substrate** through a prepreg layer (14) is carried out. Then, a semiconductor circuit element (12) is attached to the metal **substrate** frame at the mounting area by thermocompression bonding through a silver paste (12a).

An **array** of **solder balls** (17) are formed at spatial part (15a) of a solder mask layer (15) formed at the bottom. A number of metal **substrate** frames with their side rails drilled are placed side by side so that they are coupled through pilot **holes** (18a) formed using coupling tags (18c).

ADVANTAGE - Improves productivity of semiconductor device. Improves operativity such as conveyance and positioning.

Dwg.1/6

Abstract (Equivalent): US 5661086 A

A method for producing semiconductor devices comprises (a) producing a frame made of connected metal **substrates**, where connected metal **substrate** members which comprise a number of metal **substrate** members each of which have a die mounting region at a central portion of the front **surface** and which are connected in one direction by means of a number of first connecting tabs and a number of first side rails which are disposed in parallel at both sides of the metal **substrate** members and are connected with the metal **substrate** members by means of a number of second connecting tabs and are provided with a number of first positioning pilot **apertures** are formed from a copper material and subsequently an erosion preventing plating is applied to an entire **surface** of the metal **substrate** members to produce the connected metal **substrates**, (b) producing a frame made of connected circuit **substrates** by (i) a first shape forming sub step in which a number of circuit **substrate** members which are respectively provided with **openings** being aligned with the die mounting regions and are connected in one direction by means of a number of third connecting tabs and a number of second side rails which are disposed in parallel at both sides of the circuit **substrate** members and are connected with the metal **substrate** members by means of a number of fourth connecting tabs and are provided with a number of second positioning **apertures** being aligned with the first positioning pilot **apertures** formed from a **substrate** material sheet which is provided with a copper leaf on its front **surface**, (ii) a second lead pattern producing sub-step in which an etching is made on the circuit **substrate** members to provide a number of conductive leads each of which forms a wire bonding pad at the inner end and a terminal pad at an outer end, and the wire bonding pads and the terminal pads are provided with platings of a metal, (iii)

a third solder resist layer forming sub-step, in which a solder resist layer is formed on a **surface** of the conductive leads with the exception of the wire bonding pads and the terminal pads, (c) producing a frame made of connected **semiconductor die** mounting **substrates** in which the frame made of connected metal **substrates** produced in the first step and the frame made of connected circuit **substrates** produced in the second step are aligned with each other using the first and second positioning pilot **apertures** formed in the frames as reference **apertures**, a number of the circuit **substrates** are separated from the frame made of connected circuit **substrates** by removing the third and fourth connecting tabs and the separated circuit **substrates** are adhered to the metal **substrates** by means of an electrically insulating adhesive agent so as to produce the frame made of connected **semiconductor die** mounting **substrates**, and (d) producing a number of independent semiconductor devices where a **semiconductor die** is mounted in a cavity defined by each the die mounting region and each the **opening** aligned with each the die mounting portion, and a **solder ball** is welded to each the terminal pad, and the first and second connecting tabs are removed from an outer frame including the first side rails to produce the independent semiconductor devices.

Dwg.1,8/12

46/3,AB/15 (Item 15 from file: 350)  
 DIALOG(R)File 350:Derwent WPIX  
 (c) 2004 Thomson Derwent. All rts. reserv.

011014394

WPI Acc No: 1996-511344/199651

Related WPI Acc No: 1997-151806

XRAM Acc No: C96-160126

XRPX Acc No: N96-431181

**BGA** type semiconductor device for mounting onto PWB - has potting

re:in-sealing object that carries out sealing of semiconductor circuit element and bonding wire using potting resin

Patent Assignee: MITSUI HIGH TEC KK (MIHI ); MITSUI HIGH TEC INC (MIHI )

Inventor: NAKASHIMA T; TAKAI K; TATEISHI K

Number of Countries: 002 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 8264679	A	19961011	JP 9596064	A	19950328	199651 B
US 5661086	A	19970826	US 96584299	A	19960111	199740

Priority Applications (No Type Date): JP 9596064 A 19950328; JP 95136019 A 19950509

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8264679	A		5	H01L-023/12	
US 5661086	A		16	H01L-021/48	

Abstract (Basic): JP 8264679 A

The device (10) has a metal **substrate** (12) that consists of the copper system material (12b). The copper system material is covered by the nickel coating layer (12a). A mounting area (11) is provided in the metal **substrate** for a semiconductor circuit element (14). A PWB mounting **surface** (16) is formed in the junction **surface** of circuit **substrate** (17). A number of wire bonding pads (19) are arranged in the PWB mounting **surface** corresponding to a number of

electrode pads (13) on the semiconductor element. A number of terminal pads (20) are arranged in matrix shape in other end part. The circuit **substrate** is provided with a receipt **opening** part (18) of the semiconductor circuit element in central part. A solder mask (23) consisting of a solder resin is provided such that the wire bonding pad and the terminal pad are exposed.

The resin is poured on a **conductor** lead formation **surface**. A mounting **substrate** (22) carries out crimp of the circuit **substrate** to the metal **substrate** through a prepreg adhesive agent. The semiconductor circuit element is mounted through a silver paste on the mounting **substrate**. A number of **solder balls** are coupled to the terminal pads. A bonding wire is connected between the electrode pads and the bonding pads to form an electric conduction circuit. A resin sealing object (26) seals the semiconductor circuit element and the bonding wire using the resin.

ADVANTAGE - Prevents curvature, peeling of resin sealing object by heat stress. Prevents crack generation. Improves productivity and reliability at low cost.

Dwg.1/3

Abstract (Equivalent): US 5661086 A

A method for producing semiconductor devices comprises (a) producing a frame made of connected metal **substrates**, where connected metal **substrate** members which comprise a number of metal **substrate** members each of which have a die mounting region at a central portion of the front **surface** and which are connected in one direction by means of a number of first connecting tabs and a number of first side rails which are disposed in parallel at both sides of the metal **substrate** members and are connected with the metal **substrate** members by means of a number of second connecting tabs and are provided with a number of first positioning pilot **apertures** are formed from a copper material and subsequently an erosion preventing plating is applied to an entire **surface** of the metal **substrate** members to produce the connected metal **substrates**, (b) producing a frame made of connected circuit **substrates** by (i) a first shape forming sub step in which a number of circuit **substrate** members which are respectively provided with **openings** being aligned with the die mounting regions and are connected in one direction by means of a number of third connecting tabs and a number of second side rails which are disposed in parallel at both sides of the circuit **substrate** members and are connected with the metal **substrate** members by means of a number of fourth connecting tabs and are provided with a number of second positioning **apertures** being aligned with the first positioning pilot **apertures** formed from a **substrate** material sheet which is provided with a copper leaf on its front **surface**, (ii) a second lead pattern producing sub-step in which an etching is made on the circuit **substrate** members to provide a number of conductive leads each of which forms a wire bonding pad at the inner end and a terminal pad at an outer end, and the wire bonding pads and the terminal pads are provided with platings of a metal, (iii) a third solder resist layer forming sub-step, in which a solder resist layer is formed on a **surface** of the conductive leads with the exception of the wire bonding pads and the terminal pads, (c) producing a frame made of connected **semiconductor die** mounting **substrates** in which the frame made of connected metal **substrates** produced in the first step and the frame made of connected circuit **substrates** produced in the second step are aligned with each other using the first and second positioning pilot **apertures** formed in the frames as reference **apertures**, a number of the circuit **substrates** are separated from the frame

made of connected circuit **substrates** by removing the third and fourth connecting tabs and the separated circuit **substrates** are adhered to the metal **substrates** by means of an electrically insulating adhesive agent so as to produce the frame made of connected **semiconductor die** mounting **substrates**, and (d) producing a number of independent semiconductor devices where a **semiconductor die** is mounted in a cavity defined by each the die mounting region and each the **opening** aligned with each the die mounting portion, and a **solder ball** is welded to each the terminal pad, and the first and second connecting tabs are removed from an outer frame including the first side rails to produce the independent semiconductor devices.

Dwg.1,8/12

46/3,AB/16 (Item 16 from file: 350)  
 DIALOG(R)File 350:Derwent WPIX  
 (c) 2004 Thomson Derwent. All rts. reserv.

010075801

WPI Acc No: 1994-343514/199443

XRPX Acc No: N94-269549

Semiconductor device esp. wire bonded plastic encapsulated device without die support - has die bonded to **conductors** on **surface** of PCB **substrate**, with die centred in **substrate** die cavity, and has **solder balls** attached to **solder** pads connected to **conductors**

Patent Assignee: MOTOROLA INC (MOTI )

Inventor: DJENNAS F; NOMI V K; PASTORE J R; POSTLETHWAIT L; REEVES T J

Number of Countries: 007 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 623956	A2	19941109	EP 94303148	A	19940429	199443 B
EP 623956	A3	19950322	EP 94303148	A	19940429	199543
US 5474958	A	19951212	US 9355863	A	19930504	199604
JP 7321139	A	19951208	JP 94113649	A	19940428	199607
TW 264563	A	19951201	TW 94102863	A	19940401	199608

Priority Applications (No Type Date): US 9355863 A 19930504

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 623956	A2	E	19	H01L-023/498	

Designated States (Regional): DE FR GB IT

US 5474958	A	17	H01L-021/56
JP 7321139	A	14	H01L-021/60
EP 623956	A3		H01L-023/498
TW 264563	A		H01L-021/50

Abstract (Basic): EP 623956 A

The semiconductor device (120) includes a **semiconductor die** centred within a die cavity of a PCB **substrate** (100). The **substrate** has conductive traces (104) on a **substrate surface**, which extend toward the die edge. Solder pads are electrically connected to the PCB **conductors**. The die cavity has a plated sidewall (108) electrically connected to power supply **conductor** and to a corresp. solder pad. Wire bonds connect the die active **surface** to the **substrate surface conductors**.

A resin encapsulant covers the die active **surface** and the wire bonds. **Solder balls** (126) are attached to the solder

pads, for external connection. A vent **hole** (124) may be present due to a support pin used during moulding.

ADVANTAGE - Low profile, crack resistant during solder reflow; without interfaces between die support and die attach adhesive or resin encapsulant; shorter wire bond lengths.

Dwg.15/26

Abstract (Equivalent): US 5474958 A

A method for fabricating a semiconductor device comprising the steps of:

placing a **semiconductor die** having an active **surface** and a periphery on a supporting work-holder;

attaching an inactive **surface** of the **semiconductor die** to a removable tape, the tape being supported by the work-holder to rigidly hold the **semiconductor die** in a fixed position on the work-holder;

providing a first plurality of **conductors** extending toward the periphery of the **semiconductor die**;

wire bonding the active **surface** of the **semiconductor die** to the first plurality of **conductors**;

forming a package body, having planar **surfaces**, to cover the active **surface** of the **semiconductor die** and a portion of the plurality of **conductors**; and

providing a second plurality of **conductors** electrically connected to the **semiconductor die** to provide external electrical connections.

Dwg.9,19/2

02/04/2004

10/010,237

(FILE 'HOME' ENTERED AT 15:09:19 ON 04 FEB 2004)

FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 15:09:39 ON 04  
FEB 2004

L1 2 S US20030107116/PN

02/04/2004

10/010,237

(FILE 'HOME' ENTERED AT 15:09:19 ON 04 FEB 2004)

FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 15:09:39 ON 04  
FEB 2004

L1 2 S US20030107116/PN

02/04/2004

10/010,237

(FILE 'HOME' ENTERED AT 15:09:19 ON 04 FEB 2004)

FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 15:09:39 ON 04  
FEB 2004

L1

2 S US20030107116/PN

02/04/2004

10/010,237

L1 ANSWER 1 OF 2 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN  
AN 2003-645218 [61] WPIX  
DNN N2003-513302  
TI High frequency windowframe capacitor in flip-chip semiconductor package assembly, includes capacitive housing with central aperture that fits over semiconductor die on package substrate.  
DC U11 U12  
IN SEN, B K  
PA (SENB-I) SEN B K  
CYC 1  
PI US 2003107116 A1 20030612 (200361)\* 12p <--  
ADT US 2003107116 A1 US 2001-10237 20011207  
PRAI US 2001-10237 20011207  
AB US2003107116 A UPAB: 20030923  
NOVELTY - The capacitor (27) includes a capacitive housing with a rectangular central aperture that fits over a semiconductor die (11) on the package substrate (13). The capacitor is connected to the substrate using solder balls.  
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the semiconductor package assembly.  
USE - High frequency windowframe capacitor mounted using ball grid array (BGA), pin grid array (PGA), land grid array (LGA), plastic pin array (PPA) or ceramic pin grid array (CPGA) techniques on substrate of flip-chip semiconductor package assembly (claimed).  
ADVANTAGE - The overall effective capacitance is increased, while inductance is reduced. The surface area of the substrate is utilized effectively. The top area of the windowframe capacitor can be utilized for mounting additional capacitors, or voltage regulators.  
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the semiconductor package assembly.  
semiconductor die 11  
package substrate 13  
windowframe capacitor 27  
Dwg.7/8

L1 ANSWER 2 OF 2 INPADOC COPYRIGHT 2004 EPO on STN

LEVEL 1  
AN 208514791 INPADOC ED 20030630 EW 200326 UP 20031014 UW 200341  
TI WINDOWFRAME CAPACITOR.  
IN SEN BIDYUT K.  
INS SEN BIDYUT K  
INA US  
PA SEN BIDYUT K.  
PAS SEN BIDYUT K  
PAA US  
DT Patent  
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)  
PI **US 2003107116** **AA 20030612**  
AI US 2001-10237 A 20011207  
PRAI US 2001-10237 A 20011207  
OSDW 2003-645218  
AB A capacitor having an aperture in a central portion of the capacitor is provided. Such a "windowframe" capacitor has capacitive material disposed within a housing of the capacitor in order to provide effective capacitance and reduced inductance. Further, a semiconductor package assembly having a semiconductor die and a windowframe capacitor is

02/04/2004 10/010,237

provided.

02/04/2004

10/010,237

L1 ANSWER 1 OF 2 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN  
AN 2003-645218 [61] WPIX  
DNN N2003-513302  
TI High frequency windowframe capacitor in flip-chip semiconductor package assembly, includes capacitive housing with central aperture that fits over semiconductor die on package substrate.  
DC U11 U12  
IN SEN, B K  
PA (SENB-I) SEN B K  
CYC 1  
PI US 2003107116 A1 20030612 (200361)\* 12p <--  
ADT US 2003107116 A1 US 2001-10237 20011207  
PRAI US 2001-10237 20011207  
AB US2003107116 A UPAB: 20030923  
NOVELTY - The capacitor (27) includes a capacitive housing with a rectangular central aperture that fits over a semiconductor die (11) on the package substrate (13). The capacitor is connected to the substrate using solder balls.  
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the semiconductor package assembly.  
USE - High frequency windowframe capacitor mounted using ball grid array (BGA), pin grid array (PGA), land grid array (LGA), plastic pin array (PPA) or ceramic pin grid array (CPGA) techniques on substrate of flip-chip semiconductor package assembly (claimed).  
ADVANTAGE - The overall effective capacitance is increased, while inductance is reduced. The surface area of the substrate is utilized effectively. The top area of the windowframe capacitor can be utilized for mounting additional capacitors, or voltage regulators.  
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the semiconductor package assembly.  
semiconductor die 11  
package substrate 13  
windowframe capacitor 27  
Dwg.7/8

L1 ANSWER 2 OF 2 INPADOC COPYRIGHT 2004 EPO on STN

LEVEL 1  
AN 208514791 INPADOC ED 20030630 EW 200326 UP 20031014 UW 200341  
TI WINDOWFRAME CAPACITOR.  
IN SEN BIDYUT K.  
INS SEN BIDYUT K  
INA US  
PA SEN BIDYUT K.  
PAS SEN BIDYUT K  
PAA US  
DT Patent  
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)  
PI US 2003107116 AA 20030612  
AI US 2001-10237 A 20011207  
PRAI US 2001-10237 A 20011207  
OSDW 2003-645218  
AB A capacitor having an aperture in a central portion of the capacitor is provided. Such a "windowframe" capacitor has capacitive material disposed within a housing of the capacitor in order to provide effective capacitance and reduced inductance. Further, a semiconductor package assembly having a semiconductor die and a windowframe capacitor is

02/04/2004

10/010,237

provided.

EIC2800

Irina Speckhard

571 272 25 54

02/04/2004

10/010,237

L1 ANSWER 1 OF 2 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN  
AN 2003-645218 [61] WPIX  
DNN N2003-513302  
TI High frequency windowframe capacitor in flip-chip semiconductor package assembly, includes capacitive housing with central aperture that fits over semiconductor die on package substrate.  
DC U11 U12  
IN SEN, B K  
PA (SENB-I) SEN B K  
CYC 1  
PI US 2003107116 A1 20030612 (200361)\* 12p <--  
ADT US 2003107116 A1 US 2001-10237 20011207  
PRAI US 2001-10237 20011207  
AB US2003107116 A UPAB: 20030923  
NOVELTY - The capacitor (27) includes a capacitive housing with a rectangular central aperture that fits over a semiconductor die (11) on the package substrate (13). The capacitor is connected to the substrate using solder balls.  
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the semiconductor package assembly.  
USE - High frequency windowframe capacitor mounted using ball grid array (BGA), pin grid array (PGA), land grid array (LGA), plastic pin array (PPA) or ceramic pin grid array (CPGA) techniques on substrate of flip-chip semiconductor package assembly (claimed).  
ADVANTAGE - The overall effective capacitance is increased, while inductance is reduced. The surface area of the substrate is utilized effectively. The top area of the windowframe capacitor can be utilized for mounting additional capacitors, or voltage regulators.  
DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the semiconductor package assembly.  
semiconductor die 11  
package substrate 13  
windowframe capacitor 27  
Dwg.7/8

L1 ANSWER 2 OF 2 INPADOC COPYRIGHT 2004 EPO on STN

LEVEL 1  
AN 208514791 INPADOC ED 20030630 EW 200326 UP 20031014 UW 200341  
TI WINDOWFRAME CAPACITOR.  
IN SEN BIDYUT K.  
INS SEN BIDYUT K  
INA US  
PA SEN BIDYUT K.  
PAS SEN BIDYUT K  
PAA US  
DT Patent  
PIT USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)  
PI US 2003107116 AA 20030612  
AI US 2001-10237 A 20011207  
PRAI US 2001-10237 A 20011207  
OSDW 2003-645218  
AB A capacitor having an aperture in a central portion of the capacitor is provided. Such a "windowframe" capacitor has capacitive material disposed within a housing of the capacitor in order to provide effective capacitance and reduced inductance. Further, a semiconductor package assembly having a semiconductor die and a windowframe capacitor is

02/04/2004

10/010,237

provided.

EIC2800

Irina Speckhard

571 272 25 54

SYSTEM:OS - DIALOG OneSearch

File 2:INSPEC 1969-2004/Jan W4

(c) 2004 Institution of Electrical Engineers

**\*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.**

File 6:NTIS 1964-2004/Feb W1

(c) 2004 NTIS, Intl Cpyrght All Rights Res

File 8:Ei Compendex(R) 1970-2004/Jan W4

(c) 2004 Elsevier Eng. Info. Inc.

File 34:SciSearch(R) Cited Ref Sci 1990-2004/Jan W4

(c) 2004 Inst for Sci Info

**\*File 34: New prices as of 1/1/2004 per Information Provider request. See HELP RATES 34.**

File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec

(c) 1998 Inst for Sci Info

**\*File 434: New prices as of 1/1/2004 per Information Provider request. See HELP RATES434.**

File 35:Dissertation Abs Online 1861-2004/Jan

(c) 2004 ProQuest Info&Learning

File 65:Inside Conferences 1993-2004/Feb W1

(c) 2004 BLDSC all rts. reserv.

File 94:JICST-EPlus 1985-2004/Jan W4

(c) 2004 Japan Science and Tech Corp(JST)

File 99:Wilson Appl. Sci & Tech Abs 1983-2004/Dec

(c) 2004 The HW Wilson Co.

File 144:Pascal 1973-2004/Jan W4

(c) 2004 INIST/CNRS

File 305:Analytical Abstracts 1980-2004/Dec W4

(c) 2004 Royal Soc Chemistry

**\*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.**

File 315:ChemEng & Biotec Abs 1970-2004/Jan

(c) 2004 DECHEMA

File 350:Derwent WPIX 1963-2004/UD,UM &UP=200408

(c) 2004 Thomson Derwent

**\*File 350: New prices as of 1-1-04 per Information Provider request. See HELP RATES350**

File 347:JAPIO Oct 1976-2003/Sep(Updated 040105)

(c) 2004 JPO & JAPIO

**\*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.**

File 344:Chinese Patents Abs Aug 1985-2003/Nov

(c) 2003 European Patent Office

File 371:French Patents 1961-2002/BOPI 200209

(c) 2002 INPI. All rts. reserv.

**\*File 371: This file is not currently updating. The last update is 200209.**

Set	Items	Description
S1	667	AU=(SEN, B? OR SEN B?)
S2	0	S1 AND ((UNITARY OR UNIT? ?)(3N)(CAPACITOR? ? OR WINDOWFRA- M? OR WINDOW()FRAM?))
S3	5	S1 AND (CAPACITOR? ?(3N)(PLASTIC? OR STACK??? OR MOUNT????- ???? OR PILE???)
S4	3	RD (unique items)
S5	662	S1 NOT S3
S6	198	S5 AND (SUBSTRAT? OR SURFACE? OR BASE? OR SUBSTRUCT? OR UN- DERSTRUCT? OR UNDERLAY? OR FOUNDATION? OR PANE? OR DISK? OR D- ISC? OR WAFER?)
S7	1	S6 AND (BALL? ?(3N)(GRID OR ARRAY) OR BALL()GRID()ARRAY OR BGA)
S8	1	S6 AND (SEMICONDUCT??????(3N)(DIE OR DIED OR DIEING OR DIES OR DICE OR CUT OR CHOP???)
S9	1	S8 NOT S7
S10	12	S6 AND CONDUCT??????
S11	11	RD (unique items)

4/3,AB/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

5438909 INSPEC Abstract Number: B9701-2130-003, C9701-7410D-102

**Title: Performance comparison of discrete and buried capacitors**

Author(s): Sen, B.K. ; Parker, J.C., Jr.; Liou, J.-Y.; Adachi, H.; Wheeler, R.L.

Author Affiliation: Sun Microsyst. Comput. Corp., Mountain View, CA, USA

Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.2794 p.333-8

Publisher: SPIE-Int. Soc. Opt. Eng,

Publication Date: 1996 Country of Publication: USA

CODEN: PSISDG ISSN: 0277-786X

SICI: 0277-786X(1996)2794L:333:PCDB;1-M

Material Identity Number: C574-96169

Conference Title: 1996 International Conference on Multichip Modules

Conference Sponsor: SPIE; Int. Microelectron. Soc.; Int. Electron. Packaging Soc.; et al

Conference Date: 17-19 April 1996 Conference Location: Denver, CO, USA

Language: English

Abstract: The electrical performance of "on-chip" or "on-substrate" buried capacitors are compared with commercially available discrete chip capacitors mounted on the substrate. In particular, the drop in on-chip supply voltage (brown out) is studied for the internal logic switching scenario. We have assumed that only about 30% of the available noise margin is allowed for the brown out. This allowable noise margin is compared with the brown out voltages as a function of technology. It was determined that with the progress of technology, the allowable noise margin actually reduces as a percentage of the supply voltage due to short channel effects. We also observed that for slower clock frequencies, the brown out voltages are much lower than the allowed noise margin for both kinds of capacitors. At higher frequencies, the brown out voltages for the discrete chip capacitors are much higher than the allowable noise margin. The study concludes that, for a technology in the near future, and for a typical design center, discrete chip capacitors may not be sufficient. In that case, one needs to use buried chip capacitors on-substrate or on-chip for a sufficient noise margin. The main reason for this conclusion is the inductance of the discrete chip capacitors and the flight time necessary to reach these capacitors, since they have to be mounted some distance away from the chip. The conclusions of this study are based on simulation results.

Subfile: B C

Copyright 1996, IEE

4/3,AB/2 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

015583061

WPI Acc No: 2003-645218/200361

XRPX Acc No: N03-513302

**High frequency windowframe capacitor in flip-chip semiconductor package assembly, includes capacitive housing with central aperture that fits over semiconductor die on package substrate**

Patent Assignee: SEN B K (SENB-I)

Inventor: SEN B K

Number of Countries: 001 Number of Patents: 001

## Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030107116	A1	20030612	US 200110237	A	20011207	200361 B

Priority Applications (No Type Date): US 200110237 A 20011207

## Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030107116	A1	12	H01L-023/02	

Abstract (Basic): US 20030107116 A1

## Abstract (Basic):

NOVELTY - The capacitor (27) includes a capacitive housing with a rectangular central aperture that fits over a semiconductor die (11) on the package substrate (13). The capacitor is connected to the substrate using solder balls.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for the semiconductor package assembly.

USE - High frequency windowframe **capacitor** **mounted** using ball grid array (BGA), pin grid array (PGA), land grid array (LGA), plastic pin array (PPA) or ceramic pin grid array (CPGA) techniques on substrate of flip-chip semiconductor package assembly (claimed).

ADVANTAGE - The overall effective capacitance is increased, while inductance is reduced. The surface area of the substrate is utilized effectively. The top area of the windowframe capacitor can be utilized for **mounting** additional **capacitors** , or voltage regulators.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section of the semiconductor package assembly.

semiconductor die (11)  
package substrate (13)  
windowframe capacitor (27)  
pp; 12 DwgNo 7/8

4/3,AB/3 (Item 2 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

013947768

WPI Acc No: 2001-431982/200146

XRAM Acc No: C01-130611

XRPX Acc No: N01-320084

**Capacitor for filtering signal frequencies from conductive path, has two metal layers, each having multiple connections to environment**

Patent Assignee: SUN MICROSYSTEMS INC (SUNM )

Inventor: **SEN B**

Number of Countries: 001 Number of Patents: 001

## Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6252760	B1	20010626	US 99320241	A	19990526	200146 B

Priority Applications (No Type Date): US 99320241 A 19990526

## Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 6252760	B1	6	H01G-004/228	

Abstract (Basic): US 6252760 B1

## Abstract (Basic):

NOVELTY - A capacitor comprises substrate, and two metal layers, each having multiple connections to an environment.

DETAILED DESCRIPTION - A capacitor comprises a substrate, a first

interconnect layer (48) disposed upon the substrate, and a first insulating layer disposed on the first interconnect layer. A first metal layer (44) is disposed on the first insulating layer and formed as at least two regions, that are connected to the first interconnect layer through vias formed in the first insulating layer. A second insulating layer is disposed on the first metal layer. A second metal layer (42) is disposed on the second insulating layer and is formed as at least two regions. The capacitor includes a third insulating layer disposed on the second metal layer and a second interconnect layer (46) disposed on the third insulating layer and connecting to the two regions of the second metal layer through vias. A first terminal is connected to the first interconnect layer and a second terminal is connected to the second interconnect layer.

USE - For filtering signal frequencies from a conductive path.

ADVANTAGE - The invention reduces the inherent inductance while maintaining or increasing the capacitance. The capacitance is in parallel, and associated inductances are in parallel, thus providing an ideal environment for the transmission of high frequency signals.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a capacitor mounted on a package.

Second metal layer (42)

First metal layer (44)

Second interconnect layer (46)

First interconnect layer (48)

pp; 6 DwgNo 2A/4

7/3,AB/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

5769939 INSPEC Abstract Number: B9801-0170J-029

**Title: Build-up laminates used in high density applications**

Author(s): Chillara, S.; Sen, B. ; Yamamoto, K.

Author Affiliation: Fujitsu Comput. Packaging, San Jose, CA, USA

Journal: Electronic Packaging and Production vol.37, no.11 p.79-80,

82

Publisher: Cahnners Publishing,

Publication Date: Aug. 1997 Country of Publication: USA

CODEN: ELPPA5 ISSN: 0013-4945

SICI: 0013-4945(199708)37:11L.79:BLUH;1-L

Material Identity Number: E259-97010

Language: English

Abstract: Numerous organic **substrate** technologies that accommodate dense circuits and very high I/O packages are in production. They are collectively referred to as sequential build-up technologies, or simply as build-up technologies. At Fujitsu, a build-up technology in which photovias are formed on traditional laminates (such as FR-4 and BT resin) is being developed. In this approach, vias are formed by exposing and developing a photoimageable dielectric that has been applied to the core laminate. Semi-additive plating is then used to plate the vias and circuit pattern. The process is repeated to form multiple layers. This build-up technology is suitable for high-density applications such as single chip and multichip **ball grid array** /land **grid array** packages with wire bonding and flip chip, direct chip attach and chip scale packaging applications. In this article, two applications of build-up technology at Fujitsu are described: a single chip PBGA using flip chip technology and a multichip PBGA using wire bonding technology.

Subfile: B

Copyright 1997, IEE

8/3,AB/1 (Item 1 from file: 350)  
DIALOG(R)File 350:Derwent WPIX  
(c) 2004 Thomson Derwent. All rts. reserv.

009324239

WPI Acc No: 1993-017703/199302

XRPX Acc No: N93-013544

**Semiconductor device package using flexible substrate - has patterned metal layer with semiconductor die and insulating layer attached to it and moisture blocking layer on backside**

Patent Assignee: LSI LOGIC CORP (LSIL-N)

Inventor: LONG J M; MURPHY A; **SEN B** ; SIDOROVSKY R S; STEIDL M J

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5173766	A	19921222	US 90543989	A	19900625	199302 B

Priority Applications (No Type Date): US 90543989 A 19900625

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5173766	A	46	H05K-001/18	

Abstract (Basic): US 5173766 A

The semiconductor device package comprises a flexible packaging **substrate** having a patterned metal layer onto which a **semiconductor die** is attached and a patterned insulative layer attached to the metal layer. The insulative layer includes an annular epoxy-seal gap. A glob of silicone gel is deposited and cured on the die. A casting frame is connected to the metal layer of the flexible **substrate** on the same side as the die.

A backside moisture-blocking layer of material is attached to an opposed side of the tape. The frame and the backside layer are attached to the metal layer of the flexible **substrate** using cross-linkable epoxy adhesives. These epoxy adhesives join through the epoxy-seal gap to define an epoxy-seal around the die. A thermoset type of moulding compound is then poured into the casting frame to define a moisture resistance package body.

ADVANTAGE - Allows for greater pin count and densities

11/3,AB/1 (Item 1 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

7733715 INSPEC Abstract Number: C2003-10-7210-006

**Title: Research governance: implications for health library and information professionals**

Author(s): Sen, B.A.

Author Affiliation: Fac. of Bus. & Law, Liverpool John Moores Univ., UK

Journal: Health Information and Libraries Journal vol.20, no.1 p.

3-14

Publisher: Blackwell,

Publication Date: March 2003 Country of Publication: UK

CODEN: HLREEJ ISSN: 1471-1834

SICI: 1471-1834(200303)20:1L:3:RGIH;1-Y

Material Identity Number: H570-2003-001

Language: English

Abstract: The Research Governance Framework for Health and Social Care published by the Department of Health in 2001 provides a model of best practice and a framework for research in the health and social care sector. This article reviews the Department of Health Research Governance Framework, **discusses** the implications of research governance for library and information professionals undertaking research in the health- and social-care sector and recommends strategies for best practice within the information profession relating to research governance. The scope of the Framework document that covers both clinical and non-clinical research is outlined. Any research involving, amongst other issues, patients, NHS staff and use or access to NHS premises may require ethics committee approval. Particular reference is made to the roles, responsibilities and professional **conduct** and the systems needed to support effective research practice. Issues such as these combine to encourage the development of a quality research culture which supports best practice. Questions arise regarding the training and experience of researchers, and access to the necessary information and support. The use of the Framework to guide research practice complements the quality issues within the evidence- **based** practice movement and supports the ongoing development of a quality research culture. Recommendations are given in relation to the document's five domains of ethics, science, information, health and safety and finance and intellectual property. Practical recommendations are offered for incorporating research governance into research practice in ways which conform to the Framework's standards and which are particularly relevant for research practitioners in information science. Concluding comments support the use of the Research Governance Framework as a model for best practice.

Subfile: C

Copyright 2003, IEE

11/3,AB/2 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

02918390 INSPEC Abstract Number: A87080783

**Title: Modifications required on a power-compensated differential scanning calorimeter to obtain heat of adsorption measurements**

Author(s): Vannice, M.A.; Sen, B. ; Chou, P.

Author Affiliation: Dept. of Chem. Eng., Pennsylvania State Univ., University Park, PA, USA

Journal: Review of Scientific Instruments vol.58, no.4 p.647-53

Publication Date: April 1987 Country of Publication: USA

CODEN: RSINAK ISSN: 0034-6748

U.S. Copyright Clearance Center Code: 0034-6748/87/040647-07\$01.30

Language: English

**Abstract:** A commercial, power-compensated, differential scanning calorimeter (DSC) has been modified and incorporated into a gas-handling system to improve its performance and to allow its use to accurately measure heats of adsorption on supported metal catalysts. The use of gas flow controllers, needle valves, and appropriate purge gas mixtures minimized **base** -line perturbations due to uneven flow rates to the sample and references cavities and to changes in thermal **conductivity** upon introduction of the adsorbate into the purge gas. However, errors in the energy trace were still observed when large differences existed between the thermal conductivities of the adsorbate and the purge gas. These errors can be especially pronounced with processes involving the adsorption or reaction of hydrogen (if Ar is the purge gas, for example), and the severity of the problem has not previously been recognized. However, the use of a purge gas mixture with a thermal **conductivity** near that of the adsorbate minimized this problem, and employing a DSC block temperature near that of the adsorption temperature further decreased this error. Utilizing He as the purge gas allowed accurate values to be obtained for the enthalpy of Pd hydride formation and for heats of adsorption of H/sub 2/ on Pt **surfaces**. The difficulties with CO adsorption were much less severe because its thermal **conductivity** is much more similar to that of Ar, and Q/sub ad/ values for CO on Pt were more easily obtained. Finally, the error in the energy trace for H/sub 2/ when Ar was used was proportional to the amount of H/sub 2/ adsorbed; therefore a correction factor could be obtained which alternatively allowed Ar to be used as a purge gas and provided values in good agreement with those obtained under optimum conditions using He.

Subfile: A

11/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

02695888 INSPEC Abstract Number: B86042911

**Title: Impedance properties of narrow radiating slots in the broadface of dielectrically loaded rectangular waveguide**

Author(s): Sen, B. ; Ranga Rao, K.S.

Author Affiliation: Indian Inst. of Technol., Kharagpur, India

Conference Title: AP-S International Symposium 1985: Antennas and Propagation. Symposium Digest (Cat. No.85CH2128-7) p.191-4 vol.1

Publisher: IEEE, New York, NY, USA

Publication Date: 1985 Country of Publication: USA 2 vol. vi+862 pp.

U.S. Copyright Clearance Center Code: CH2128-7/85/0000-0191\$01.00

Conference Sponsor: IEEE

Conference Date: 17-21 June 1985 Conference Location: Vancouver, BC, Canada

Language: English

**Abstract:** The formulation of the normalized admittance of a radiating slot in the broadface of a dielectrically loaded thin-walled rectangular waveguide is presented. The derivation is **based** on a concept introduced by J. Van Bladel (Proc. IEEE, vol.118, p.43-50, Jan. 1971) for a radiating aperture in a plane of two different media. The normalized resonant **conductance** has been found to be almost the same as that obtained using the Babinet principle. The resonant length, computed with the present formulation, is independent of slot displacement. However, variation of the resonant length with slot displacement can be observed if the stored energy inside the guide due to slot field is taken into account in determining the

slot admittance.

Subfile: B

11/3,AB/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

(c) 2004 Institution of Electrical Engineers. All rts. reserv.

02683459 INSPEC Abstract Number: A86076230

Title: **Mechanism of proton transport in HUP (HUO/sub 2/.PO/sub 4/.4H/sub 2/O)**

Author(s): **Sen, B.K.** ; Sen, S.

Author Affiliation: Dept. of Chem., Univ. Coll. of Sci., Calcutta, India

Journal: Solid State Ionics, Diffusion & Reactions vol.18-19, pt.2

p.1025-9

Publication Date: Jan. 1986 Country of Publication: Netherlands

CODEN: SSIOD3 ISSN: 0167-2738

U.S. Copyright Clearance Center Code: 0167-2738/86\$03.50

Conference Title: Solid State Ionics - 85. Proceedings of the 5th International Conference

Conference Date: 18-24 Aug. 1985 Conference Location: Lake Tahoe, NV, USA

Language: English

Abstract: Existing theories for the mechanism of proton transport in HUP has been considered and their limitations **discussed**. The crystal structure of the material has been examined. The transport of protons from one water square to another might take place through the participation of the pi-charge cloud of the phosphate group. A suitable rotation of the water molecule provides the continuous proton pass. The variation of **conductivity** with temperature and pressure have been interpreted.

Subfile: A

11/3,AB/5 (Item 1 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

(c) 2004 Elsevier Eng. Info. Inc. All rts. reserv.

02282894

E.I. Monthly No: EIM8710-072456

Title: **MECHANISM OF IONIC TRANSPORT IN POLYMERIC SOLID ELECTROLYTES: A NEW APPROACH.**

Author: **Sen, B. K.** ; Sen, S.

Corporate Source: Univ Coll of Science, Calcutta, India

Conference Title: Transport-Structure Relations in Fast Ion and Mixed Conductors, Proceedings of the 6th Riso International Symposium on Metallurgy and Materials Science.

Conference Location: Roskilde, Den Conference Date: 19850909

E.I. Conference No.: 09461

Source: Proceedings of the Riso International Symposium on Metallurgy and Materials Science 6th. Publ by Riso Natl Lab, Roskilde, Den p 347-352

Publication Year: 1985

CODEN: PRISEA ISSN: 0108-8599 ISBN: 87-550-1137-3

Language: English

Abstract: The ion transport mechanism of the alkali metal salt complexes of polyethylene oxide (PEO) is **discussed**. The generally accepted idea that **conduction** is due to movement of cations from site to site along the core of the helical structure does not agree with experiments. In PEO, the mutual coulombic repulsion of the lone pairs forces them to orient themselves outwards the helical strands. A polyhelical structure for these complexes is proposed in which the lone pair electrons on the oxygen atoms

'coordinate' to the alkali cations. In a dynamically disordered medium, the configurational motion of the polymeric framework will lead to the freedom of some of these lone pairs of suitably placed strands to allow for a transient low potential pathway for one dimensional motion of the cations. The model has been applied to explain experimental findings including variation of **conductance** with temperature, pressure, concentration of salt and heat treatment. (Edited author abstract) 12 refs.

11/3,AB/6 (Item 2 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

(c) 2004 Elsevier Eng. Info. Inc. All rts. reserv.

02034937

E.I. Monthly No: EI8610102757

E.I. Yearly No: EI86111930

Title: **MECHANISM OF PROTON TRANSPORT IN HUP (HUO//2 X (TIMES) PO//4 X (TIMES) 4H//2O).**

Author: **Sen, B. K.** ; Sen, S.

Corporate Source: Univ Coll of Science, Calcutta, India

Source: Solid State Ionics v 18-19 pt 2 Jan 1986, Solid State Ionics - 85, Proc of the Int Conf, Lake Tahoe, CA, USA, Aug 18-24 1985 p 1025-1029

Publication Year: 1986

CODEN: SSIOD3 ISSN: 0167-2738

Language: ENGLISH

Abstract: Existing theories for the mechanism of proton transport in HUP has been considered and their limitations **discussed**. The crystal structure of the material has been examined. The transport of protons from one water square to another might take place through the participation of the pi-charge cloud of the phosphate group. A suitable rotation of the water molecule provides the continuous proton pass. The variations of **conductivity** with temperature and pressure have been interpreted. (Author abstract) 14 refs.

11/3,AB/7 (Item 3 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

(c) 2004 Elsevier Eng. Info. Inc. All rts. reserv.

01409944

E.I. Monthly No: EI8312099647

E.I. Yearly No: EI83011060

Title: **REPROCESSING OF SPENT HIGH TEMPERATURE SHIFT CATALYST OF THE Fe//2O//3-Cr//2O//3 TYPE.**

Author: Hoque, S. N.; Chabra, D. S.; **Sen, B.**

Corporate Source: Fertilizer (Planning and Development) India Ltd, Sindri, India

Source: Indian Journal of Technology v 20 n 12 Dec 1982 p 493-497

Publication Year: 1982

CODEN: IJOTA8 ISSN: 0019-5669

Language: ENGLISH

Abstract: Attempts have been made to reprocess the sintered Fe//2O//3-Cr//2O//3 type high temperature shift catalysts **discharged** after 2-3 years of operation in plant by adding regenerating agents and giving physicochemical treatments to develop the physical properties like **surface** area, porosity, total pore volume, pore size distribution and particle size **conductive** to catalyst activity. The activity of reprocessed catalysts has been found to be dependent on the amount of fresh iron oxide in the catalyst mass. The physical properties cited above do not bear any relationship with the activity recovered except that the **surface**

area has a bearing on the initial activity. Ammonium dichromate and nitric acid are good regenerating agents and gum and starch poison the catalyst. The stability of activity of the catalysts is also good. 23 refs.

11/3,AB/8 (Item 1 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
(c) 2004 Inst for Sci Info. All rts. reserv.

07981864 Genuine Article#: 232KH Number of References: 40

**Title: Permeability changes of dentine treated with titanium tetrafluoride**  
(ABSTRACT AVAILABLE)

Author(s): Kazemi RB (REPRINT) ; Sen BH ; Spangberg LSW

Corporate Source: UNIV CONNECTICUT,CTR HLTH, SCH DENT MED, DEPT RESTORAT  
DENT & ENDODONTOL, 263 FARMINGTON AVE/FARMINGTON//CT/06030 (REPRINT);  
EGE UNIV,SCH DENT, DEPT RESTORAT DENT & ENDODONTOL/IZMIR//TURKEY/

Journal: JOURNAL OF DENTISTRY, 1999, V27, N7 (SEP), P531-538

ISSN: 0300-5712 Publication date: 19990900

Publisher: ELSEVIER SCI LTD, THE BOULEVARD, LANGFORD LANE, KIDLINGTON,  
OXFORD OX5 1GB, OXON, ENGLAND

Language: English Document Type: ARTICLE

Abstract: Objectives: The aim of this research was to evaluate the effect of titanium tetrafluoride on dentine permeability in comparison with sodium fluoride and acidulated phosphate fluoride to determine their contribution to acid resistance of dentine.

Methods: Thirty-two dentine **discs** were prepared from extracted mandibular molars. The hydraulic **conductance** of all **discs** was measured before and after the formation of smear layer. The **discs** were then randomly divided into five experimental and one-control groups. Coronal **surfaces** of dentine **discs** were treated with either fluoride solutions of NaF, APF, 1% TiF<sub>4</sub>, 0.5% TiF<sub>4</sub> and 0.1% TiF<sub>4</sub> or de-ionised water. Following the measurement of hydraulic **conductance**, treated **surfaces** were subjected to 25% citric acid application. Then, final permeability measurements were made. The data were statistically analysed using ANOVA and Tukey's HSD multiple comparisons.

Results: While smear layer formation considerably reduced dentinal permeability of dentine **discs**, fluoride or de-ionised water application to smeared **surfaces** did not cause any significant change in hydraulic **conductance** ( $p > 0.05$ ). After citric acid application, control and NaF groups showed higher permeability values than 1%, 0.5% and 0.1% TiF<sub>4</sub> and APF groups ( $p < 0.01$ ).

Conclusion: Clinical use of acidic solutions of titanium tetrafluoride in dentine cavities may be considered since smeared dentine **surfaces** are modified to a stable and acid-resistant state.  
(C) 1999 Elsevier Science Ltd. All rights reserved.

11/3,AB/9 (Item 2 from file: 34)

DIALOG(R)File 34:SciSearch(R) Cited Ref Sci  
(c) 2004 Inst for Sci Info. All rts. reserv.

01586585 Genuine Article#: HJ889 Number of References: 12

**Title: MODELING OF THE HEAT-TRANSFER PROCESS IN A DIFFERENTIAL SCANNING CALORIMETER** (Abstract Available)

Author(s): SEN B

Corporate Source: BIRLA INST TECHNOL & SCI,DEPT CHEM ENGN/PILANI  
333031/RAJASTHAN/INDIA/

Journal: AICHE JOURNAL-AMERICAN INSTITUTE OF CHEMICAL ENGINEERS, 1992, V38  
 , N3 (MAR), P438-444

Language: ENGLISH Document Type: ARTICLE

Abstract: The model developed predicts a priori potential errors associated with the energy trace recorded by an isoperibol differential power scanning calorimeter in the measurement of heat of adsorption of H-2 on Pt and Pd catalysts. The uptake of H-2 by the catalyst sample was approximated by a diffusion-limited quasi-steady-state moving boundary model. This approximation is valid only if the parameter [(adsorption capacity of cat. sample)/(inlet conc. of H-2)] is extremely large (approximately 24). The effect of flow rate, amount of H-2 adsorbed, sink temperature, and the thermal **conductivity** of the adsorbate mixture was examined. Model predictions indicate that the error in the energy trace recorded by the DSC is appreciable: if a large difference exists between the thermal **conductivity** of the inert carrier, Ar ( $k = 0.017 \text{ J/m.K.s}$ ), and the adsorbate, H-2 ( $k = 0.174 \text{ J/m.K.s}$ ); if the heat sink temperature is much lower (approximately 90 K) than the measurement temperature. However, these errors can be eliminated by matching the thermal **conductivity** of the inert carrier and adsorbate, such as He ( $k = 0.143 \text{ J/m.K.s}$ ) and H-2 ( $k = 0.174 \text{ J/m.K.s}$ ). The results agree well with the experimental observations of Vannice et al. (1987) on high-purity Pt and Pd powder and supported Pt catalysts, if the H-2 uptake by the catalyst sample in the calorimeter is small (less-than-or-equal-to  $2\text{-}\mu\text{mol}$ ).

11/3,AB/10 (Item 1 from file: 35)

DIALOG(R)File 35:Dissertation Abs Online

(c) 2004 ProQuest Info&Learning. All rts. reserv.

01462213 AADAAI9603955

**EFFECTS OF INJECTION HOLE GEOMETRY, HIGH FREESTREAM TURBULENCE, AND SURFACE ROUGHNESS ON FILM COOLING HEAT TRANSFER**

Author: **SEN, BASAV**

Degree: PH.D.

Year: 1995

Corporate Source/Institution: THE UNIVERSITY OF TEXAS AT AUSTIN (0227)

Source: VOLUME 56/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL.

PAGE 5698. 143 PAGES

This dissertation reports an investigation of compound angle injection, **surface** roughness, and freestream turbulence effects on film cooling heat transfer. Including **surface** roughness and freestream turbulence effects makes the study more realistic, as gas turbine operation is characterized by rough blade **surfaces** and high freestream turbulence. This is a major contribution of this study. Two different  $CA = 0^\circ$  geometries, with different hole spacing, length, and inclination, and two different compound angle levels, were studied. One of the compound angle geometries had an expanded exit. The effects of two different **surface** roughness levels were compared to the smooth **surface**. The results for a freestream turbulence level of 20% were compared to low freestream turbulence results.

All the tests were **conducted** at a density ratio of unity. Temperatures were measured on smooth or rough constant heat flux **surfaces** downstream of injection, for a zero acceleration flat plate flow, to determine heat transfer coefficients. Results are presented as  $h_{\text{f}}/h_{\text{sb0}}$ , the ratio of the film cooling heat transfer coefficient to the heat transfer coefficient at the same location without injection, and as NHFR, a measure of overall film cooling performance, derived by combining  $h_{\text{f}}/h_{\text{sb0}}$  with adiabatic effectiveness ( $\eta$ ) results

from Schmidt (1995).

The results showed that for  $CA = 0^\circ$  injection,  $h_{f}/h_{0}$  was essentially 1.0, so  $\eta$  determined NHFR. Compound angle injection increased  $h_{f}/h_{0}$ , and consequently, reduced NHFR despite improvement in  $\eta$  over  $CA = 0^\circ$  holes. **Surface** roughness increased the heat transfer without film cooling ( $h_{0}$ ) by up to 60% over the smooth **surface**. The relative effect of film cooling on heat transfer for smooth and rough **surfaces** was not significantly different. High freestream turbulence levels caused an increase in  $h_{0}$  of about 30% over the low freestream turbulence case. Combining roughness and high freestream turbulence caused the greatest increase in  $h_{0}$ . For  $CA = 0^\circ$  holes, freestream turbulence did not change  $h_{f}/h_{0}$ , but for compound angle injection it was lower than at low turbulence for all **surfaces**. Both **surface** roughness and high freestream turbulence caused a degradation in NHFR (by about 50% and 30%, respectively).

11/3,AB/11 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

(c) 2004 Thomson Derwent. All rts. reserv.

012139487

WPI Acc No: 1998-556399/199847

XRAM Acc No: C98-166436

XRFX Acc No: N98-433738

**Capacitor manufacture for multi chip module applications - comprises forming a dielectric layer over a conductive layer, forming conductive pads, testing the capacitor structures to find any defective capacitance, and forming second conductive layer over the pads**

Patent Assignee: FUJITSU LTD (FUJIT )

Inventor: PETERS M G; **SEN B K** ; WANG W V; WHEELER R L

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5817533	A	19981006	US 96692800	A	19960729	199847 B

Priority Applications (No Type Date): US 96692800 A 19960729

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 5817533	A	12	H01L-021/00	

Abstract (Basic): US 5817533 A

Forming a capacitor comprises: (a) forming a dielectric layer (16) over a first **conductive** layer (14); (b) forming a number of **conductive** pads (18) over the dielectric layer; each pad forms a capacitor structure with the dielectric layer and the first **conductive** layer; (c) testing the capacitor structures to find any defective capacitance; and (d) forming a second **conductive** layer (40) over the pads such that this layer is electrically isolated from pads of defective capacitor structures (19).

USE - For forming high-valued capacitors for multi-chip module applications.

ADVANTAGE - High-valued capacitor with high yield are provided. Fabrication procedures are compatible with common semiconductor fabrication procedures. Large embedded bypass capacitors in MCM **substrates** are obtained with minimal impact to the overall manufacturing yield and cost.

Dwg.11/12

**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

**BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**